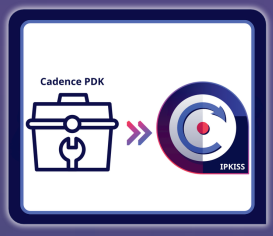
LUCEDA PHOTONICS

Luceda E/O Co-Design Integration for Cadence

Luceda E/O Co-Design Integration for Cadence offers a powerful workflow from photonic synthesis to physical and functional verification, accelerating your electro-optical IC development. By bridging Luceda's Python-driven photonic synthesis with Cadence's gold-standard EPDA ecosystem, this integration helps you eliminate manual transfer errors and reduce time-to-market for large-scale co-integrated electronic and photonic ICs.



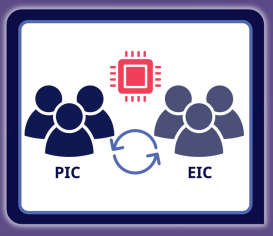
Use native Cadence PDK cells to directly implement the IPKISS Layout.



Leverage Luceda's full curvilinear design capabilities, as well as verification with Irys DRC.

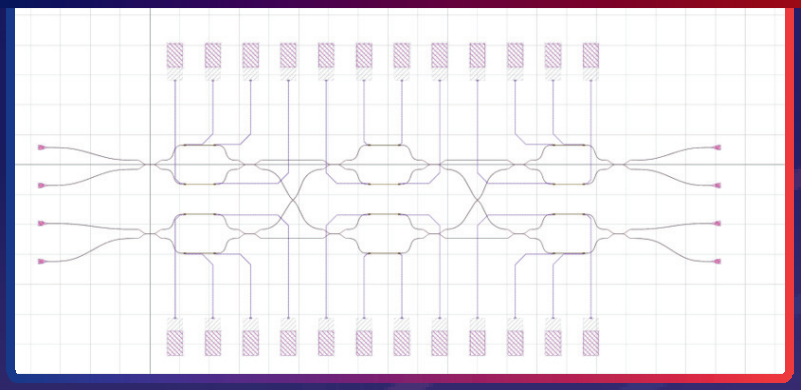


Export from IPKISS to the Cadence Virtuoso platform, with 1:1 cell & metadata matching.

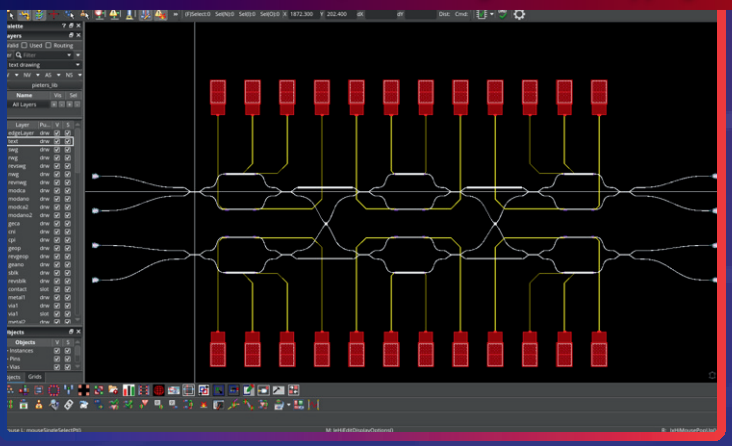


Align PIC & EIC design teams to co-design in lockstep.

Beneš switch layout in IPKISS, leveraging Luceda's specialized photonic synthesis.



Export layout to Cadence Virtuoso Studio, maintaining PDK cell mapping and metadata.



TRY IT TODAY!

Scan the QR code to learn more about Luceda E/O Co-Design Integration for Cadence, request a demo or access.

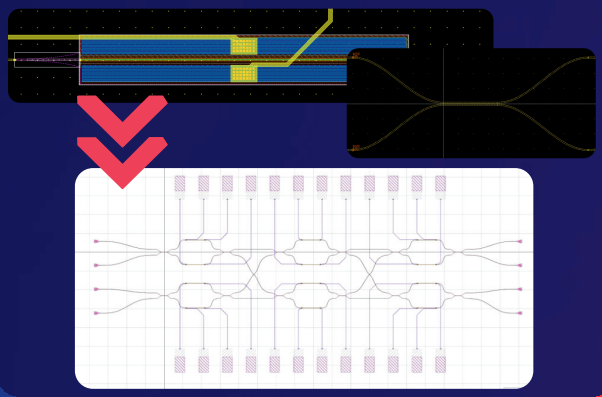
SCAN ME

www.lucedaphotonics.com

Luceda E/O Co-Design Integration for Cadence

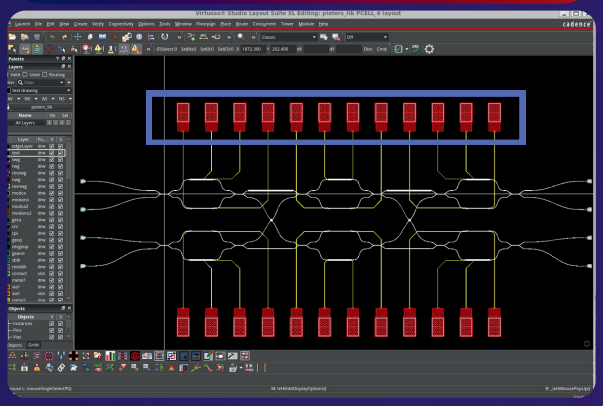
Enable electro-optical system integration by bridging Luceda's Python-driven photonic synthesis with Cadence's gold-standard EPDA ecosystem.

PDK Import & 1:1 Mapping



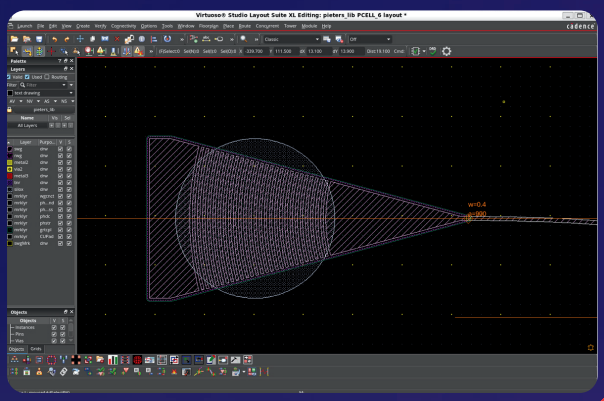
- Import Cadence PDKs or custom libraries with 1:1 mapping of cells, parameters, and metadata.
- Synthesize and build complex PIC designs within Luceda using Cadence native PDK components.

Constraint-Aware PIC Layout



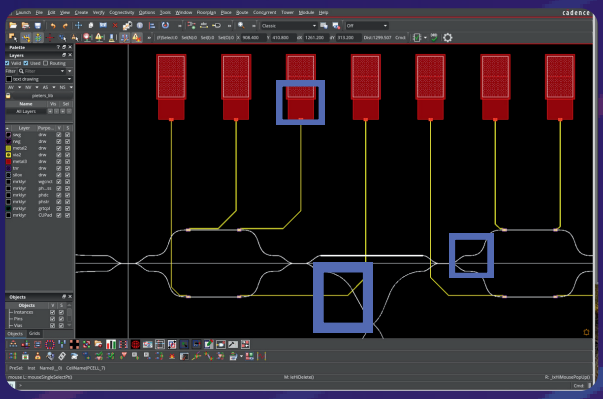
- Import layout constraints directly from the Electronic Integrated Circuit (EIC) layout.
- Account for EIC constraints during PIC layout to ensure error-free electro-optical co-design.

IP Generation & Design Export



- Create PIC IP in Luceda and transfer it to Cadence Virtuoso to complete your circuit.
- Export PIC designs back to Cadence with 1:1 mapping of cells, parameters, and metadata.

Electro-Optical Verification



- Photonic DRC: Resolve design rule violations early using Irys DRC directly inside Luceda.
- System Verification: Execute LVS and CAS within Cadence to ensure system functionality.

BENEFITS

For PIC Designers

- Eliminate manual file transfer errors and ad-hoc scripting.
- Identify & resolve optical-specific design rule violations early in Irys DRC.
- Leverage specialized PIC design and analysis capabilities.
- Work in a flexible, open EPDA design environment.

For EIC Designers

- Easier PIC–EIC collaboration in your preferred design environment.
- Share layout requirements and constraints across design environments.
- Combine PIC and EIC designs for tape-out-ready Cadence verification.

For Foundries

- Reduce engineering effort for cross-platform PDK development and maintenance.
- Effortlessly translate PDKs between Cadence and Luceda to expand your customer base.

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