SHIFT LEFT
THE EDA JOURNAL

ISSUE 1 – FALL 2024

Enabling Enterprise Digital Transformation

Design Innovation | Workflow Automation | Engineering Productivity

KEYSIGHT

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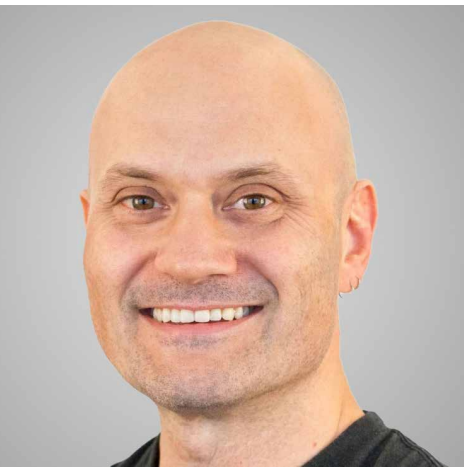


Letter from the Editor

Welcome to the first issue of *SHIFT LEFT*, the Keysight EDA Journal. Why are we doing this? Because electronic design is hard and slow - but it doesn't always have to be. Learning from Keysight EDA customers, as well as our own internal test equipment engineering teams, leads to unique insights that significantly improve EDA workflows, user productivity, and expertise. This Journal is our new vehicle for delivering that value to engineering teams and managers. In it you'll find educational technical articles and videos that discuss the latest design practices as well as real-world application case studies, and more.

The demands and complexity of electronic product development in turn drive the "A" in EDA - Automation. But design automation as it is traditionally thought of is far removed in some ways from what is possible today. Yes, you can script repetitive tasks, you can scale up your compute resources, and you can learn about faster ways to create and deploy models. Yet there are also new ways for engineering teams to collaborate, leverage IP, and parallelize human processes. This Journal goes beyond just traditional EDA, because many workflow improvements can be realized only through deeply understanding the broader engineering context. This includes new trends in electronics manufacturing, data management, and processes.

Wouldn't you love to reduce busy work and get back to what we as engineers really love to do - engineering? It's tragic that many of us in design and verification roles are spending upwards of 50% of our paid work time doing documentation, compliance tracking, or resolving conflicts. Sure, there's a place for managing tasks and organizing projects and priorities. But if you're anything like me, you got into this because you have a passion for advancing technology, so what keeps you from doing more of that? THAT is where THIS Journal is designed to help YOU. We realized there's a need for experts in electronics to have a trusted source of knowledge that is technical in nature, which can lift everyone's game through learning about new practical approaches, and help you evolve as a technology leader and adopter.

SHIFT LEFT is designed to show you what's new in multiple domains across the electronics engineering and EDA landscape, from a transformative and practical standpoint. Sure, you'll learn what new products are coming from Keysight EDA from time to time. But the true aim is to pro-

vide techniques, key insights, and industry learning from experts in RF, Signal and Power Integrity, Devices, Circuits, System Design, Power Electronics, and Data & IP Management. Our goal for *SHIFT LEFT* is that with each issue you will learn something new which you can apply immediately, that will make your role as an engineer, engineering manager, or technology leader more productive. You'll hear from industry leaders inside Keysight as well as from those outside the company.

Why is this new Journal called "*SHIFT LEFT*"? It might be tempting to think that it is named such because an arithmetic shift left is equivalent to multiplication. Indeed, we want the content in this publication to multiply yours and your team's productivity, but that's not the reason. At Keysight, to "*SHIFT LEFT*" means to take what used to be sequential, delayed and disparate processes in the engineering lifecycle, and by leveraging accurate digital "twins," perform multiple stages in parallel. In a visual representation of a linear process it means shifting those stages to the left as depicted in Figure 1.

In addition to technical articles and industry trends, we think you'll find *SHIFT LEFT* to be mentally stimulating. We want to provoke positive change in your daily engineering practice and in the industry at large, so you'll see a reader challenge, interviews with fascinating people, and hear the voice of Keysight users. And I humbly request that you take the time to offer your honest feedback - each issue will have a form you can use to quickly share your evaluation and comments, as well as offer suggestions for new articles and topic requests for future editions.

I personally find the topics in this first edition helpful and illuminating, and I am certain you will too.

Ben Jordan, Editor

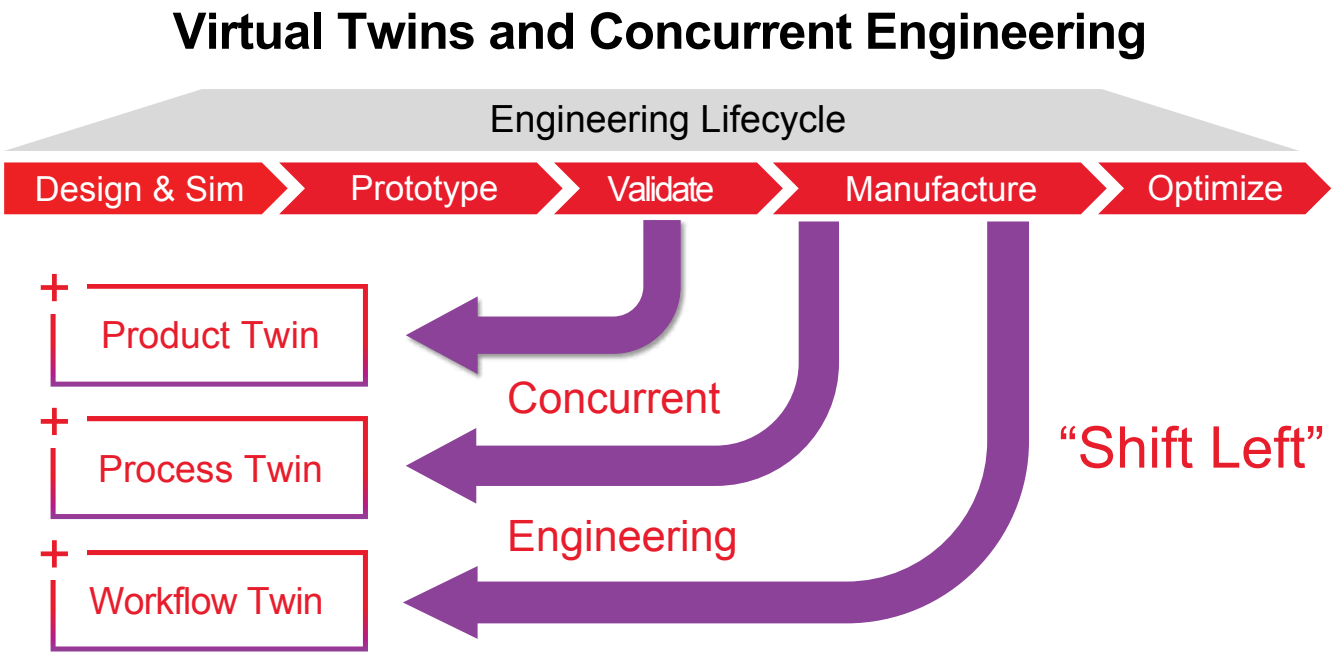
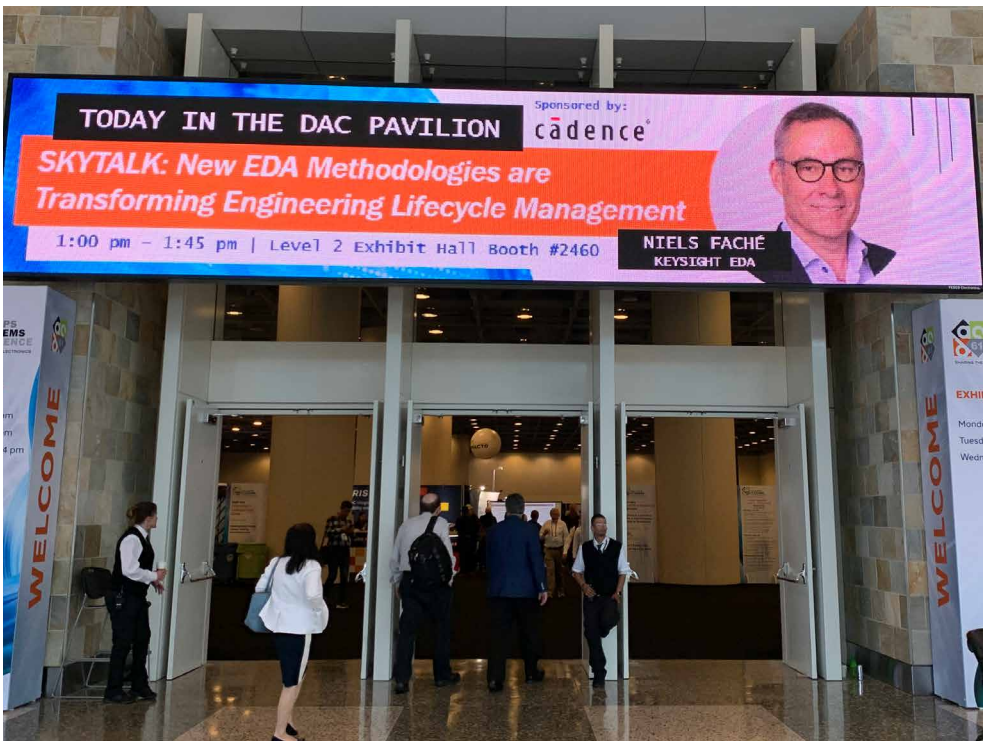


Figure 1: Shift left is the term for Concurrent Engineering.
(Source: Niels Faché's DAC 61 "SKYtalk" - See the featured video on page 7).

How New EDA Methodologies Are Transforming Engineering Lifecycle Management

Watch this SKYTalk presentation by Keysight VP & GM for EDA, Niels Faché, to learn how tools and workflows are rapidly evolving to overcome challenges such as coping with exploding system complexity and delivering multi-disciplinary solutions. He covers a broad range of topics—from how digital process twins improve product verification by 20-50 percent to rapid adoption of AI in the EDA industry. The discussion also explains why predictive simulation and analysis across domains is key to accelerating engineering lifecycles. In addition, as the industry deals with ever-greater device complexity, effective data and IP management strategies become vital for protecting intellectual assets, fostering innovation, and maintaining a competitive edge in rapidly evolving markets.

You will also learn why teams need new workflows such as tools and methodologies for emerging technologies like 3D ICs and photonics communications subsystems. More importantly, Niels explains how sys-



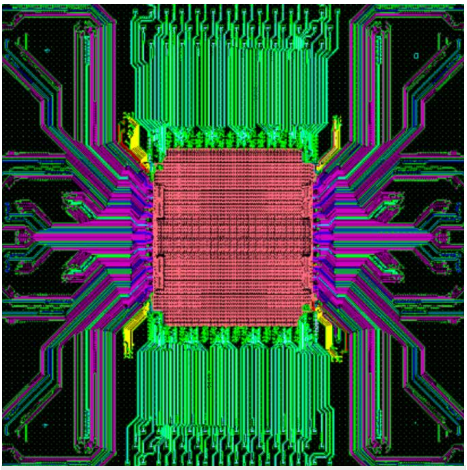
tem-level design comprises a collection of application-specific workflows having a high degree of specialization. However, advances in technology reveal a number of shortcomings inherent in these workflows:

- Tools may lack capabilities to handle new applications
- Tools often lack automation for the problem at hand
- Generic simulation technology is slow and may not provide predictive results

Nonetheless, application-specific workflows are key to transforming engineering lifecycle management. Keysight's vision for differentiating these solutions from generic workflows includes:

- Built-in Application Expertise – Provides the right capabilities and guided experience for the job
- Built-in Automation – Shortens the engineering effort
- Best-in Class Technology (enabled by an open ecosystem) – Provides predictive results for multi-physic effects
- Digital threads – Connect virtual prototypes and digital twins with physical arms of the process V-model

This transformation is key to how EDA is shifting-left connected workflows and reshaping engineering lifecycle management.



Case Study

Organization:

- Sarcina Technology LLC

Challenges:

- Ease of Use
- ASIC Package Design
- Dense, High-Power Devices
- Chip-Package-Board Signal Integrity > 100 Gbps

Solutions:

- Advanced Design System (ADS); SI/PI Pro
- ADS Memory Designer
- IBIS-AMI Simulation Model Integration

Results:

- Simulation Accuracy
- DDR6 and 112 GbE PAM-4 Package Success
- Significant Cost Savings

Sarcina Delivers Right-First-Time Packages Using ADS For Chip-Package-Board Simulation

Semiconductor package engineering has a unique set of challenges that make it difficult for fabless semiconductor companies to win first-time success. Packages come in many different materials and topologies, suited for different applications such as medical, aerospace, automotive, consumer electronics, etc. Converging on an optimal package design for complex semiconductors such as CPU/GPU/NPU has evolved into a highly specialized practice.

Sarcina Technology LLC, headquartered in Palo Alto with a presence in Taipei, Taiwan, is one such semiconductor package design service. Established in 2011, Sarcina has carved a niche in designing semiconductor packages for some of the most sophisticated devices in the market. Their prowess is showcased in their work on workstations and datacenter CPUs, GPUs, and network processors that employ the latest technologies.

As a premier "wafer-in, package-out" service provider, they adeptly incorporate the latest standards for interconnect, such as DDR6, PCIe Gen 6, SERDES, and 100 Gbps (and faster) Ethernet. Many of the semiconductor dice they cater to are true powerhouses, drawing hundreds of watts during peak operation. Packages designed by Sarcina have found their way into diverse sectors, ranging from consumer electronics to space endeavors like the Falcon 9 mission to the ISS in May 2020.

Sarcina has proven themselves by achieving first-time successful tape-out time and time again. Larry Zu, Sarcina's CEO, says the company possesses deep advanced semiconductor package design experience. Larry sheds light on the company's strategic use of Keysight's ADS for their groundbreaking chip-package-board channel simulations.

Challenges: Accurate Signal Path Analysis

Semiconductor packages, especially those used with modern high-performance and high-bandwidth devices, form a critical part of the overall signal path. Take a high-end network processor for example, a signal comes in from an internal silicon gate, then travels along a silicon-metal

"The customer gives us the semiconductor wafers from TSMC or Global Foundries or Samsung. Then we do wafer bumping, sorting, package design, electrical and thermal simulations. We next tape out the package, manufacture the substrate, do the assembly and final test. We send the customer assembled packages to do their lab evaluation, and ultimately ship the product."

Larry Zu

transmission line, to a bump or chip bond pad, then through the package to the host motherboard. There are vias and transmission lines throughout each of these sections and transitions between them. All of these transitions and vias are opportunities for electrical signal degradation and must be optimized.

Sarcina designs the package by analyzing the entire signal path from chip, to bump, to package, to board, to connector and all along the line to the receiving device. This adds significant complexity to the configuration of traditional SPICE-based tools, making for very slow progress. Sarcina package design methodology features full channel simulation. The challenge is to enable accurate, fast simulation using real-world models, without slowing down the engineering team.

Initially, Sarcina tried industry-standard SPICE-based simulation tools. The company immediately encountered difficulty: lack of good user interfaces among tools, and the need for a lot of text-based model configuration. Sarcina's engineers wanted a tool that would focus more on the task at hand and maintain model accuracy without getting bogged down in scripting.

Accuracy is critically important for simulation of chip packages and essential for achieving first-time package tape-out success. Accurate simulation of chip packages and the PCB channel is necessary for feeding back Signal Integrity / Power Integrity (SI/PI) performance into design changes that make the system work within the necessary margins.

Most of the cost of package design lies in required multiple engineering disciplines: layout, manufacturing, signal and power integrity, EMC, and test. Simulation traditionally has been the bottleneck to getting package designs finalized and ready for production, in large part due to extended simulation runs that consume days of computing. Sarcina needed an EDA tool that would accelerate simulation and provide their engineers overnight results.

Due to the cutting-edge nature of package design around new (unreleased) silicon, signal speeds, and voltage levels are being used which have not been used before. It's therefore necessary to be able to integrate additional model and parameter extraction methods and tools, using the resulting data in the main simulator without having to modify it. Moreover, it's desirable to have the ability to create brand-new models based upon the silicon designer's input.

Solution: End-to-End Workflow for Productivity

Sarcina developed a detailed workflow for end-to-end package design services, centered around simulation. Traditional package and interconnect designers tend to only address signal integrity at the PCB level, but by adopting ADS and the multi-model signal path approach, Sarcina's results

accurately represent the real-world signal characteristics. ADS is the backbone of this workflow for simulation because it is the easiest to use and most accurate for such complex tasks. Power Integrity is also challenging in such small areas where power dissipation can be hundreds of watts (Figure 1).

To accurately simulate an entire channel, the physical layout of the package signal paths, connectors,

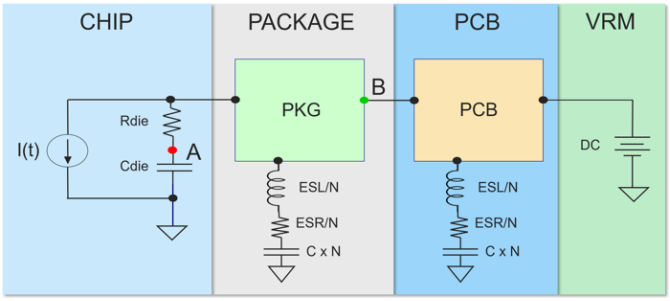


Figure 1. End-to-End PI analysis.

"You know, at 54 Gbps data rate and with bi-directional simulation, we can validate not only the silicon but also the package and the PCB."

Larry Zu

and PCB traces are all extracted using a 3D electromagnetic solver. The resulting frequency domain S-Parameter files are then used to precisely replicate the transfer function of each critical signal path. ADS uses S-Parameters with great efficiency by converting S-Parameter files into time domain impulse response (IR) coefficients, which are convolved with the input stimulus during simulation.

Accurate simulation requires covering the entire channel, as depicted in Figure 2. This example demonstrates DDR channel simulation that involves several interconnect structures which normally introduce reflections and crosstalk. By simulation of the entire end-to-end channel, Sarcina is able to pinpoint every location in the package design that must be modified to reduce impedance discontinuities.

In one example, Sarcina developed a cost-effective package for a network processor. Multiple channels had to be designed fitting 20 SerDes lanes, 8 PCIe Gen 3 lanes, and 3733 MT/s 32-bit LPDDR4 – all into a 23mm x 23mm 480-ball FCBGA package. This required the package to have a 2-2-2 layer stack. This is no easy task given that the package also must include enough capacitance on-board to meet power integrity requirements.

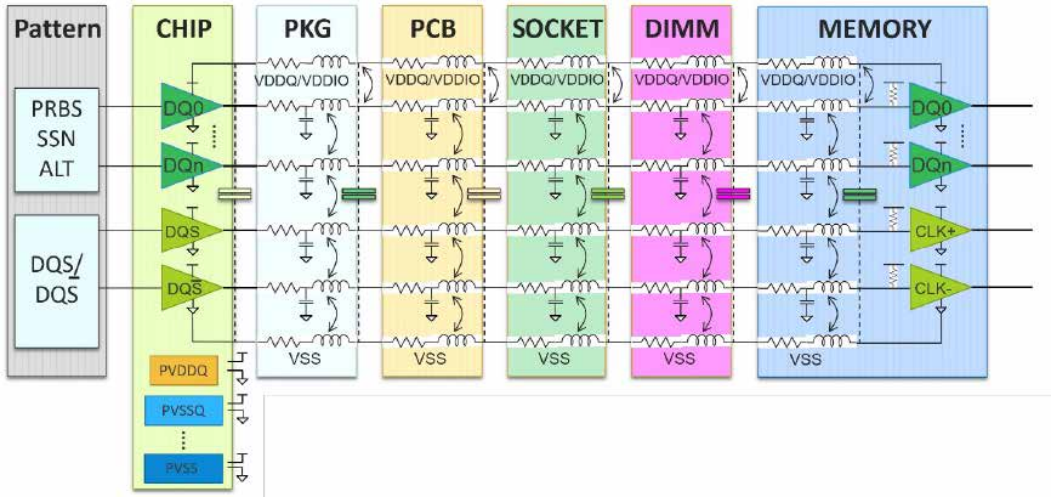


Figure 2. LPDDR5 detailed channel analysis schema.

To achieve first-time success, Sarcina uses ADS along with:

- IBIS-AMI models of new silicon provided by the IP Vendor
- S-parameter EM extractions from the package substrate and routing
- Transient PRBS (Pseudo-Random Bit Sequence) and DC simulation sources

Design requirements are provided in terms of allowable channel loss vs frequency, voltage high and low levels, BER (Bit Error Rate), and power supply tolerance (Figure 3). Sarcina uses this as input to configure ADS for SI/PI simulation, as well as output graph generation and pass/fail analysis.

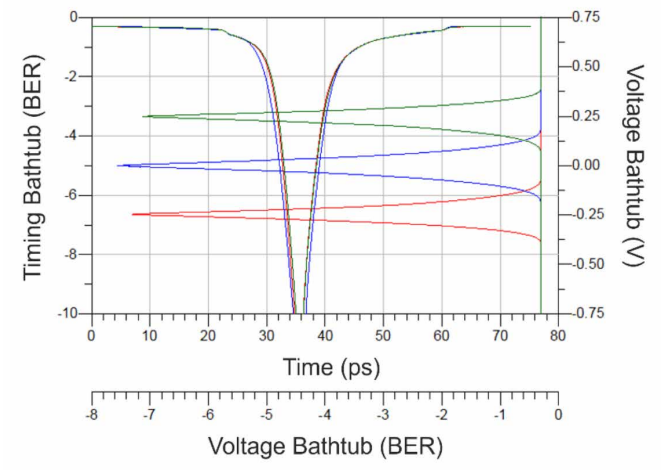


Figure 3. BER requirements overlayed on voltage bathtub.

In high-speed digital systems, multi-level signaling increases throughput on lossy PCB and package substrates without increasing the Nyquist frequency (symbol rate). Standards like PCIe Gen 6 and 100 Gbps Ethernet all require this and adopt PAM4 (Phase/Amplitude Modulation, 4-Level). PAM4 offers the best currently available data throughput within signal-to-noise ratio (SNR) and channel loss budgets.

Sarcina designs packages for the latest semiconductors and employs ADS with the latest IBIS-AMI models and signal sources. Using the built-in simulation libraries and models from the semiconductor IP vendors, they integrate modern high-speed modulated signaling. This enables accurate results, and a clear view as to how package design elements (as shown in Figure 4) physically impact modulation and can cause issues such as unbalanced eyes, offset, SNR, and jitter.

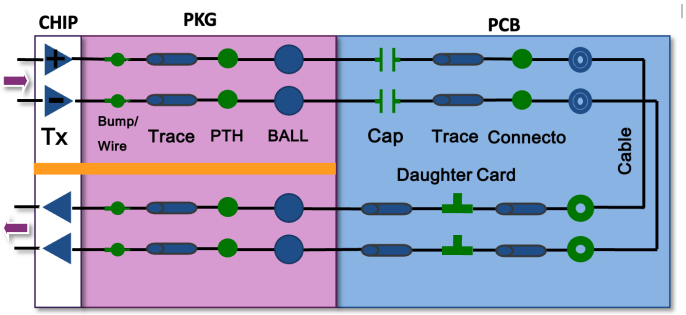


Figure 4. 56 Gb/s PAM4 topology of Network Processor

Sarcina selected ADS as their central simulation tool. Their engineering team evaluated alternatives and made a unanimous decision based on productivity.

> *"The engineers love the interface, the ease-of-use of ADS."*
>
> **Larry Zu**

The Sarcina team wanted a system that had an intuitive graphical user interface with rich model libraries. The block-based design approach, with each item in the signal chain being configurable through wizards and dialogs that are designed with the end user in mind, made the team productive immediately. ADS came out on top for performance, accuracy, and ease of use.

"Based on the scale of our simulations, getting convergence can be a big challenge. We're not just simulating a few components. We're dealing with hundreds of components, so the accuracy, and resolving SPICE convergence issues are very important."

Larry Zu

Results: Simulation Matches Measurements

Sarcina has a 100% success rate for all of the package designs using ADS at the heart of their workflow. Accuracy is particularly important and includes every element of the signal and power distribution network on each package.

Traditional loadboard design analysis focuses on PCB layout, but fails to include package, connector, and cable effects. ADS allows easy integration of the entire signal chain, including external component S-Parameter and IBIS-AMI models. This allowed Sarcina to accurately test the entire system before committing the loadboard design to manufacturing.

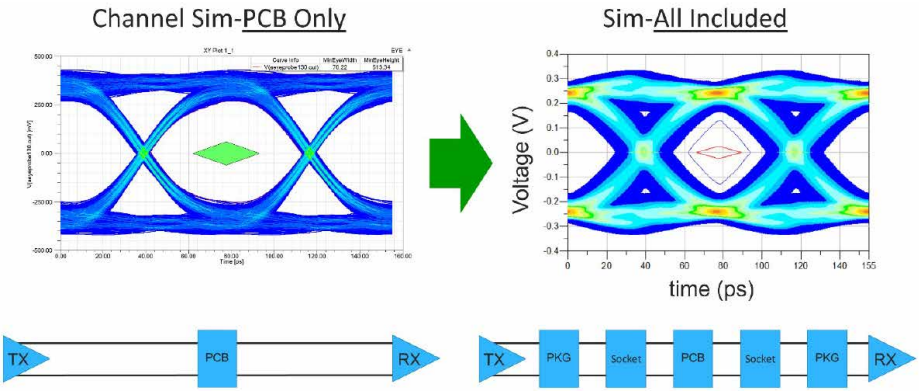


Figure 5. Simulation accuracy afforded by ADS

Figure 5 compares the ADS simulation results. This compares favorably to the measurement on Keysight instruments in the customer's lab. The ADS simulation, when set up with the right parameters and models, produces results that correlate very precisely with real-world measurements.

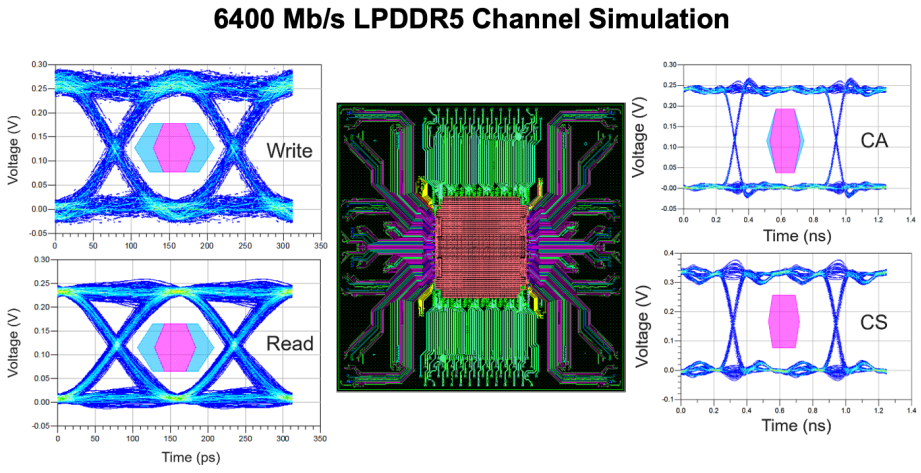


Figure 6. Results of LPDDR5 SI with network processor

Another example case is a high-speed NPU. Sarcina created an advanced package design that utilized 6400 MT/s LPDDR5 memory. Configuring the package layer stack, power and ground references, and routing according to the electrical requirements, enabled Sarcina to create a first-time success with a very demanding signaling scheme in a fraction of the time it would take using other tools (Figure 6).

By importing cutting-edge IBIS-AMI models from silicon IP vendors, Sarcina performed accurate bi-directional analysis on the LPDDR5 interconnects. Different devices on the interconnect have different signal drive strengths. The results of performing these simulations in ADS and Memory Designer show that with the correct driver and termination settings for the die, signal integrity across the package is maintained and there is plenty of eye margin.

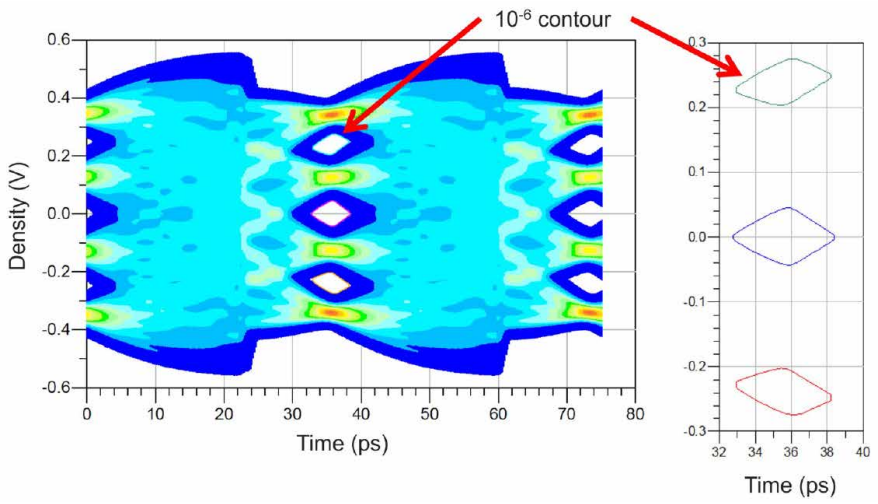


Figure 7. PAM4 eye masks for 56 Gb/s channel

"We did a measurement with Keysight test equipment. We captured an eye diagram from the measured computer screen and compared it against the simulation result. We positioned them one on top of each other and they were practically identical."

Larry Zu

Another case cited by Sarcina is 56 Gbps Ethernet, consisting of two differential channels paired and using PAM4 modulation.

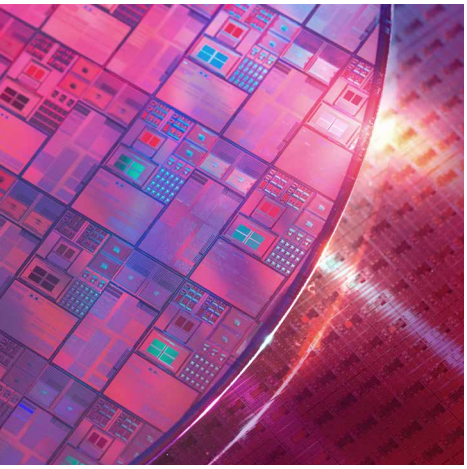
Using the customer's requirements, Sarcina specifies the eye contours for channel simulation that yield bit error rate (BER) demands. Figure 7 shows the eye contour created in ADS that met the specified targeted performance. The graph is the simulation result after 1.5 million bits of PAM4 PRBS data were simulated.

Sarcina saves cost

By integrating ADS and Memory Designer into the complete package design, simulation, die-bond, and bring-up test workflows, Sarcina specializes in this unique and difficult task. Some semiconductor start-ups hire their own package engineering staff. While this can work well for simpler devices, more often than not, fabless semiconductor start-ups do not have the skill set or resources to take on the challenge.

A typical packaging team includes a power integrity simulation engineer, a signal integrity simulation engineer, a package layout engineer, a manager to manage the team with knowledge and experience in this niche, and close relationships with two packaging factories to mitigate supply chain risk. Sometimes, a thermal/mechanical engineer and an assembly process engineer are also needed.

The annual cost for this team, including human resources and software, is close to $2 million. Although the cost in China drops to $1 million, it's not financially possible to support such a team because start-ups usually tape out only one chip every two years. In other words, the team would be idle more than half the time. Sarcina, however, accomplishes the job with a fraction of the budget, saving hundreds of thousands of dollars for every advanced package.



Using the Device Model Generator Re-Centering Tool in IC-CAP

What is Model Recentering?

Model recentering is an indispensable step in semiconductor device modeling. Engineers use recentering to adjust existing model libraries to meet new fabrication targets and specifications as the semiconductor manufacturing process evolves. Rather than starting the modeling process from scratch, recentering allows engineers to adjust previously extracted model parameters to match the new specs or measured data. As semiconductor process specifications mature, modeling teams must quickly update model libraries to match them. Thus, it becomes challenging to maintain up-to-date models with effective recentering.

To simplify the recentering process, the Recentering Tool has been developed in the IC-CAP Model Generator (MG). Traditional recentering involves a lot of repetitive tasks which, apart from being slow and tedious, can lead to error. To save time and improve model quality, the recentering tool automates these tasks.

Using the Recentering Tool, new targets and their statistical distributions are imported. The trend plots showing simulations vs. targets can be displayed for extracting parameters. This tool also allows the modeling engineers to turn on corner simulations and display the simulated corner traces along with the typical or nominal curve being tuned/optimized.

To begin model recentering in IC-CAP MG, transistor models from the current library are used as a reference point. Typically, updated values for Figures-of-Merit (FoM) are provided. They are measured at different die sizes and temperatures. These updated FoM represent the new targets as the process has changed. Recentering involves tuning and optimization techniques to adjust important model parameters to align the model with the new targets. The Model Generator with Recentering Tool allows for real-time visualization to adjust trend plots. As a result, modeling teams can save up to 70% of their time in this process by simulating data points efficiently across different geometries and temperatures.

Another critical use case of recentering is Target Modeling. In this scenario, measured data such as DC, IV curves, and S-parameters, are unavailable. Therefore, the model is extracted directly from process target information, a common practice at the early stages of the process development cycle. An earlier version of the model is extracted so circuit designers can begin application designs earlier on in the cycle. The model is then refined and recentered as more data, including measurements, become available.

In this application note, the Model Generator Recentering Tool is described in detail with a BSIM-CMG example.

Model Generator Recentering Tool

The IC-CAP Model Generator Recentering Add-on allows you to recenter an existing model or a subcircuit based on new Figures-of-Merit (FOM) targets. While model recentering can be applied to an existing MG project in which the model was extracted using IV, CV, or S-parameter measurements, recentering can also be applied when only targets are available.

There is a recentering example with the BSIM_CMG model in Model Generator; it can be opened by clicking on start MG... > Open Example > ICMG_BSIM_CMG_Recentering_Example.icproj.

The step of recentering modeling for VTLIN, ILIN_norm, and ION versus length are shown in Figure 1. The symbols represent the typical values for each length, where the blue line is the current simulation result, and the pink line is the previous simulation result. Referring to Figure 1, in the Extract stage, expand Task 1 then right-click on Step 3, as shown in the red dashed box. All the details, such as selected recentering plots, parameters, algorithm, and tuning options, will be added. So, the key point in the process is how to achieve such graphs quickly. The Recentering Tool provided in Model Generator can realize this need without additional coding.

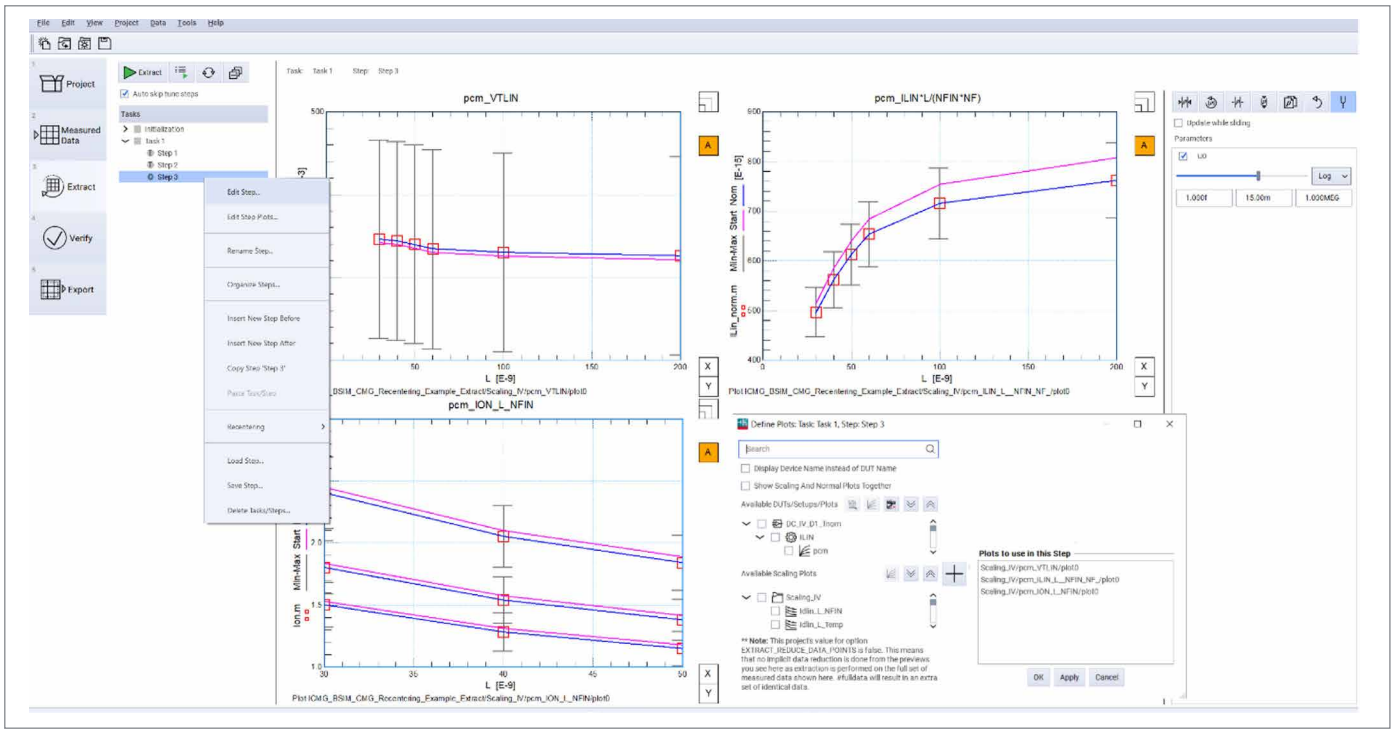
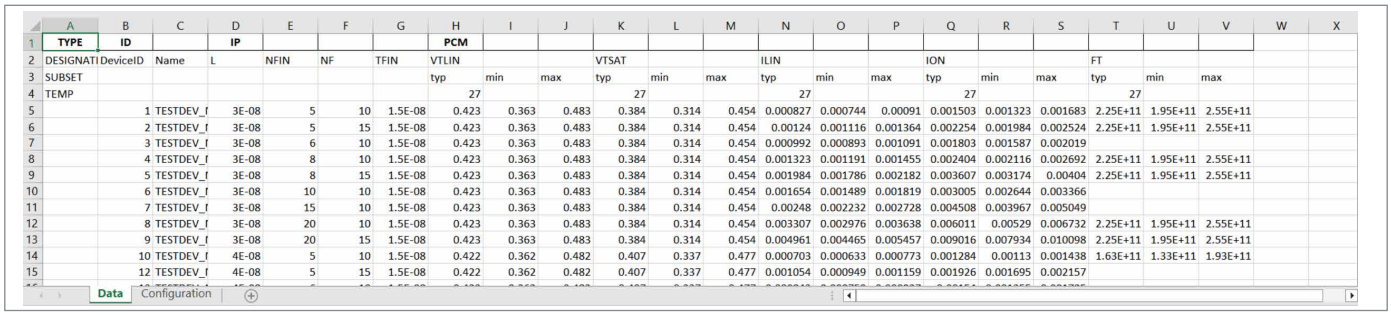


Figure 1. The step of recentering a model in IC-CAP Model Generator.

Format Data for Recentering Tool

The data for the Recentering Tool needs to be tabulated into a standard format, and another configuration table is needed for importing the necessary information, such as the needed Figures of Merit, sweeping conditions, error function, error limit, etc.

Figure 2 (a) shows the data format, and (b) shows the configuration for the Recentering Tool. The spreadsheet "ICMG_BSIM_CMG_PCM_Data.xlsx" can be found in the example folder. The details of the data table are shown in Table 1, and the configuration table is shown in Table 2.



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12		8	TESTDEV_I	3E-08	20	10	1.5E-08	0.423	0.363	0.483	0.384	0.314	0.454	0.003307	0.002976	0.003638	0.006011	0.00529	0.006732	2.25E+11	1.95E+11	2.55E+11		
13		9	TESTDEV_I	3E-08	20	15	1.5E-08	0.423	0.363	0.483	0.384	0.314	0.454	0.004961	0.004465	0.005457	0.009016	0.007934	0.010098	2.25E+11	1.95E+11	2.55E+11		
14		10	TESTDEV_I	4E-08	5	10	1.5E-08	0.422	0.362	0.482	0.407	0.337	0.477	0.000703	0.000633	0.000773	0.001284	0.00113	0.001438	1.63E+11	1.33E+11	1.93E+11		
15		12	TESTDEV_I	4E-08	5	15	1.5E-08	0.422	0.362	0.482	0.407	0.337	0.477	0.001054	0.000949	0.001159	0.001926	0.001695	0.002157					

Data | Configuration

(a)

	A	B	C	D	E	F	G	H	I	J	K	L
1	MeasurementType	PCM	FOM	ERROR_FUNC	ERROR_LIMIT	ERROR_UNIT	vg_con	vg_start	vg_stop	vg_step	vd_con	freq_con
2	TargetIV	ION	id	(Model/Target-1)	2	%	1				1	
3		ILIN	id	(Model/Target-1)	2	%	1				0.1	
4		VTSAT	vth_idref	(Model-Target)	10			-0.5	1	0.01	1	
5		VTLIN	vth_idref	(Model-Target)	10			-0.5	1	0.01	0.1	
6	TargetSP	FT	fT	(Model/Target-1)	15	%	1				0.5	1E+10
7												

(b)

Figure 2. (a) The table with data format, and (b) The table of configuration for use in the Recentering Tool.

Table 1

Variable	Description
TYPE	Type of variables, including designation, subset, and temperature
ID	Device ID and name
IP	Instance parameters
PCM	Process Control Monitoring (PCM) data In this example, there are five PCM data: VTLIN, VTSAT, ILIN, ION, and FT Under each PCM, there are three subsets: typ – typical data, min – minimum data, max – maximum data

Table 2

Variable	Description
Measurement Type	IV, SP, or CV
PCM	Process Control Monitoring data
FOM	Figure of Merit for calculating PCM data
ERROR_FUNC	Error function used for calculating errors shown in Error Summary
ERROR_LIMIT	Error limit used in Error Summary
ERROR_UNIT	Error unit used in Error Summary
Sweep condition	The bias/frequency for FOM simulation

Creating Recentering Plots

Once the spreadsheet is ready, the recentering plots are created using Scaling Plots. This is done by first creating the necessary geometry groups as shown in Figure 3.

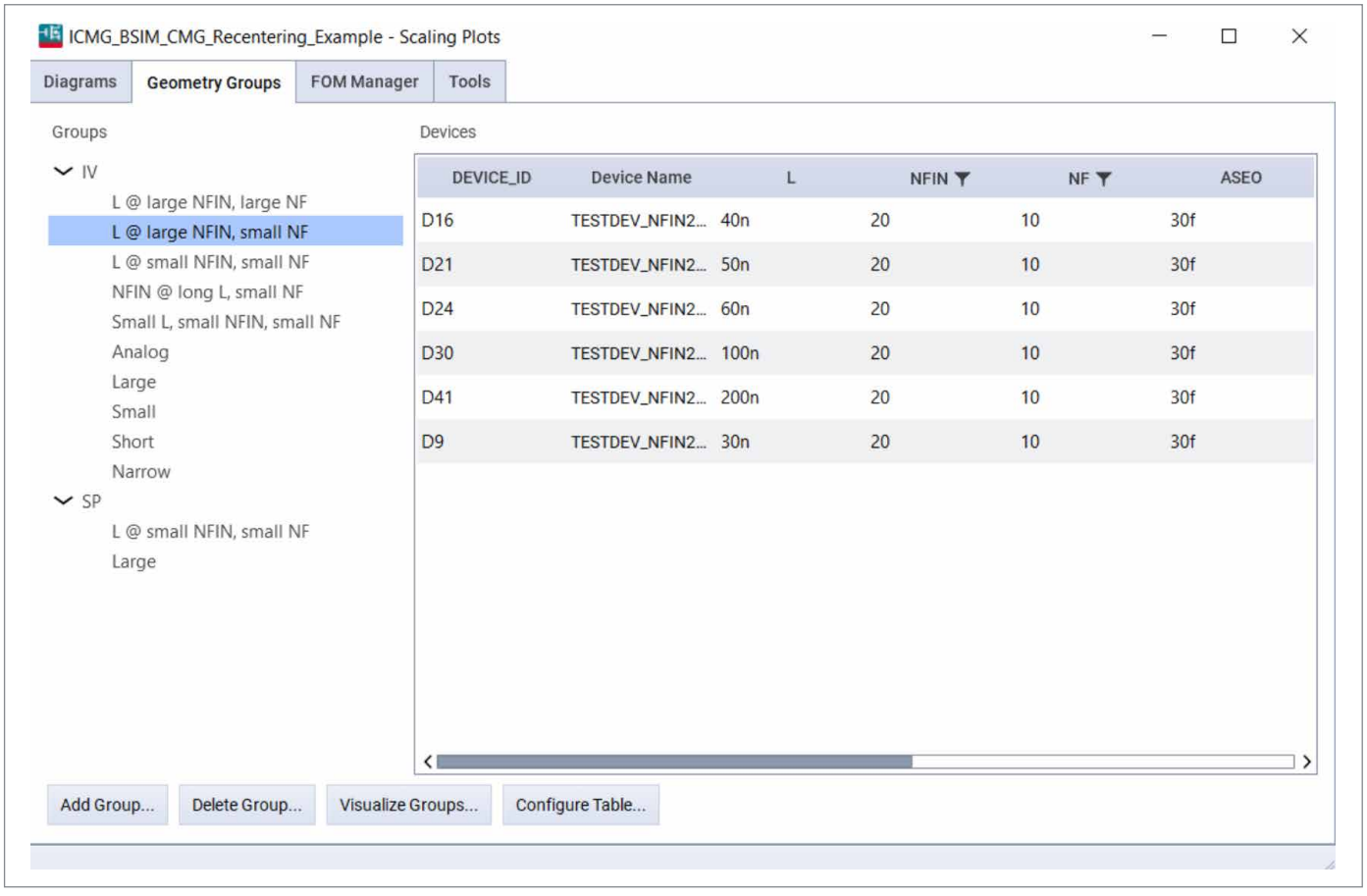


Figure 3: Create geometry.

Second, import the spreadsheet containing the recentering data and configuration shown in Figure 2 by using Tools>Recentering>Import Targets... (see Figure 4).

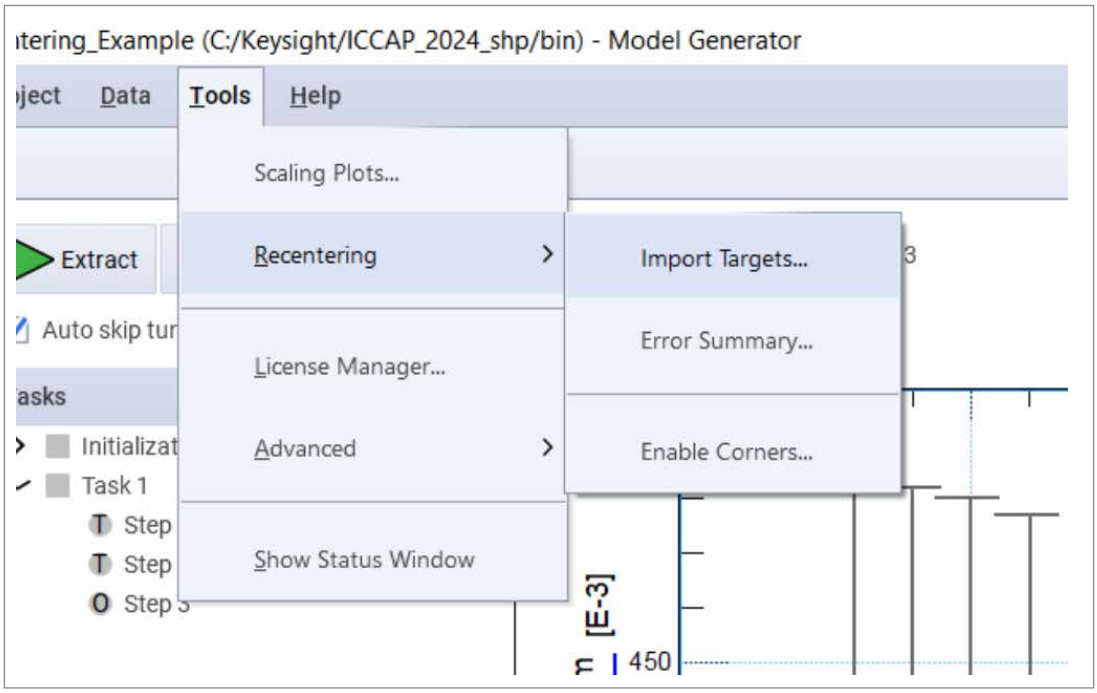


Figure 4. Import targets and configuration for recentering modeling into Model Generator.

The import status can then be seen from the IC-CAP status window, as shown in Figure 5.

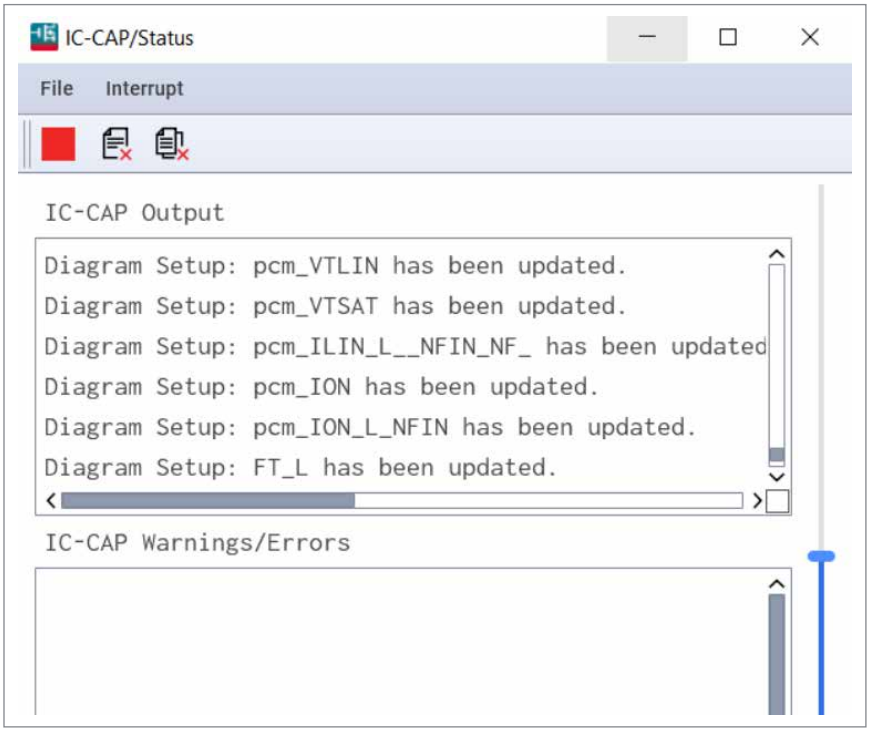


Figure 5: Status after import of recentering data

Upon importing the target and configuration into IC-CAP, the Figure of Merits will be automatically generated, as shown in Figure 6. Unlike regular FOM, the PCM or target FOM are fully defined in the spreadsheet, so there is no need to select bias or frequency information.

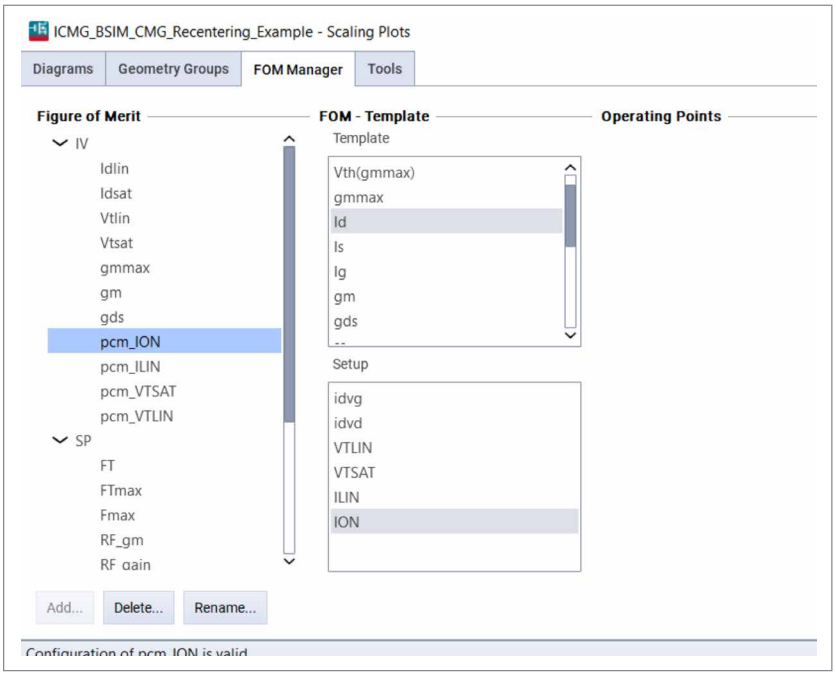


Figure 6: The Figure of Merits are automatically created.

Finally, configure the diagrams as demonstrated in Figure 7. These recentering plots can now be easily used by selecting them from the Edit >Step > Plots... (as previously shown in Figure 1 at the beginning), and the corresponding parameters are then tuned.

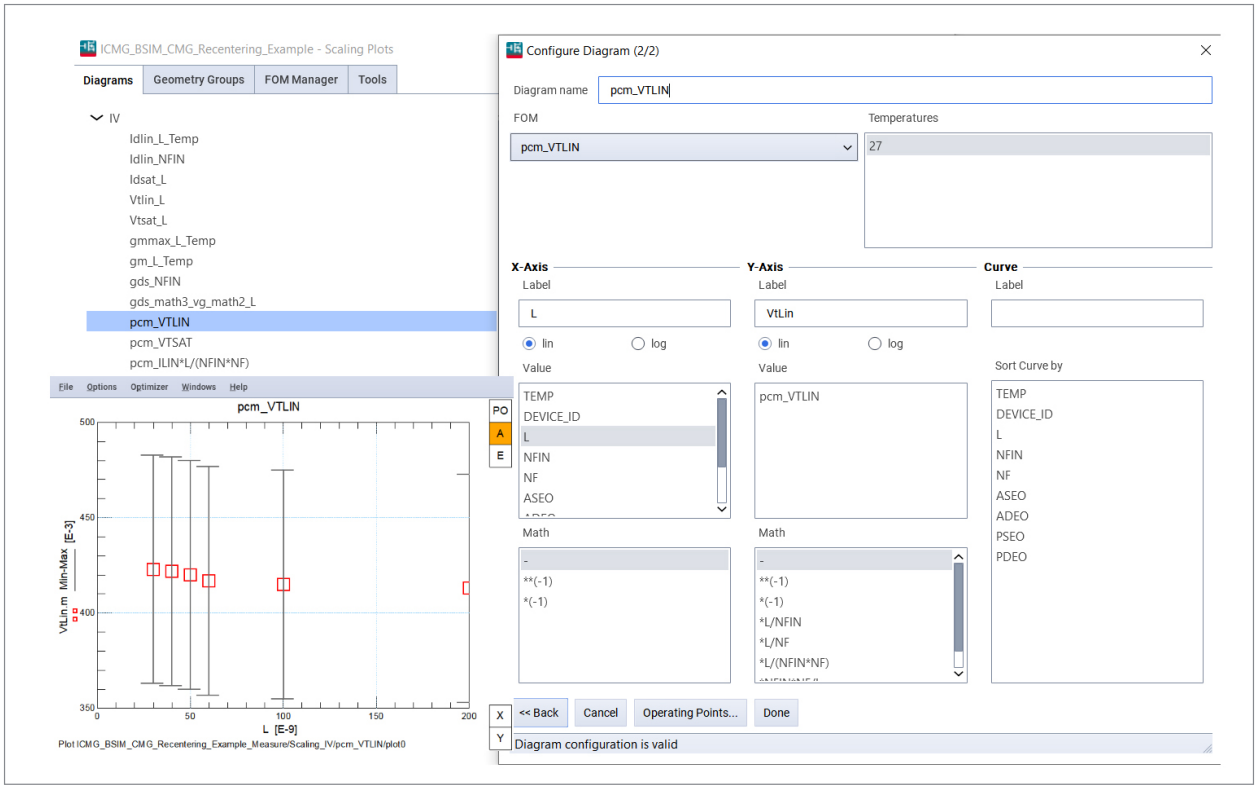


Figure 7: Configure the diagrams and check the plots

When turning on Enable Corners... under the Recentering Tool, the simulation results of the four corners, FF, SS, FS, and SF can be seen in the plots, as shown in Figure 8. By adjusting the corresponding parameters, the corner can be made to achieve the new targets.

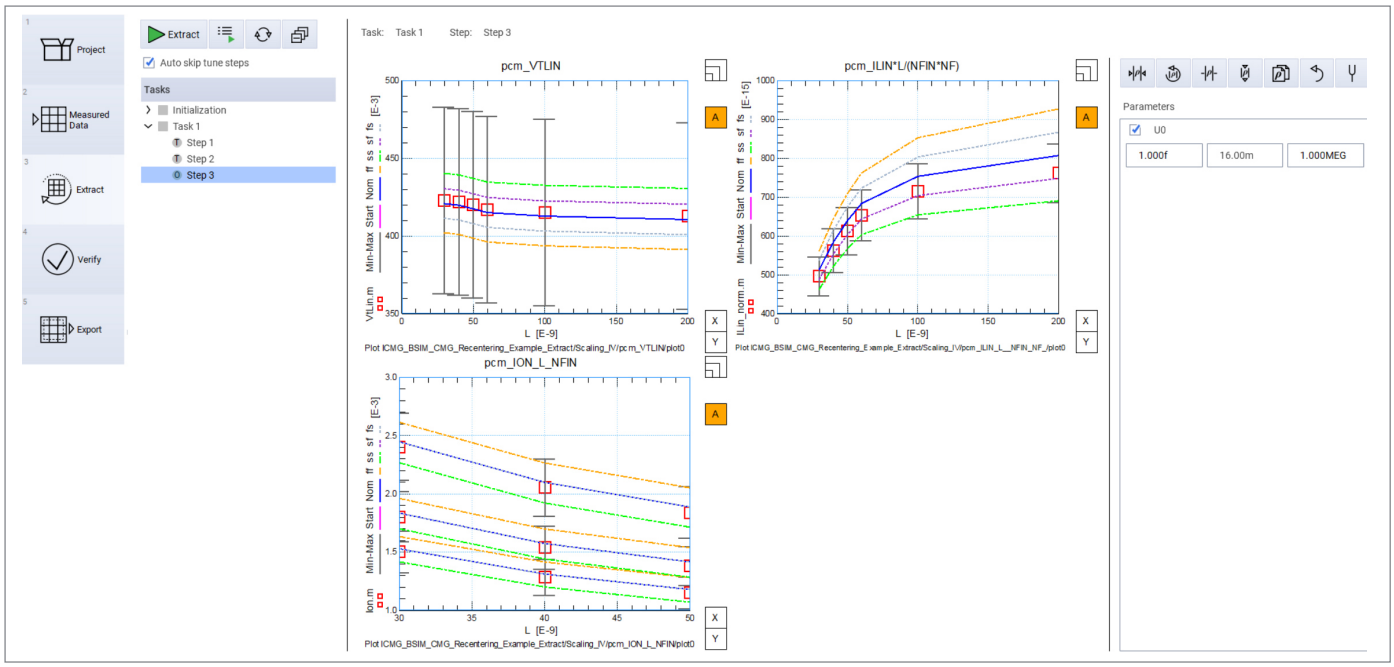
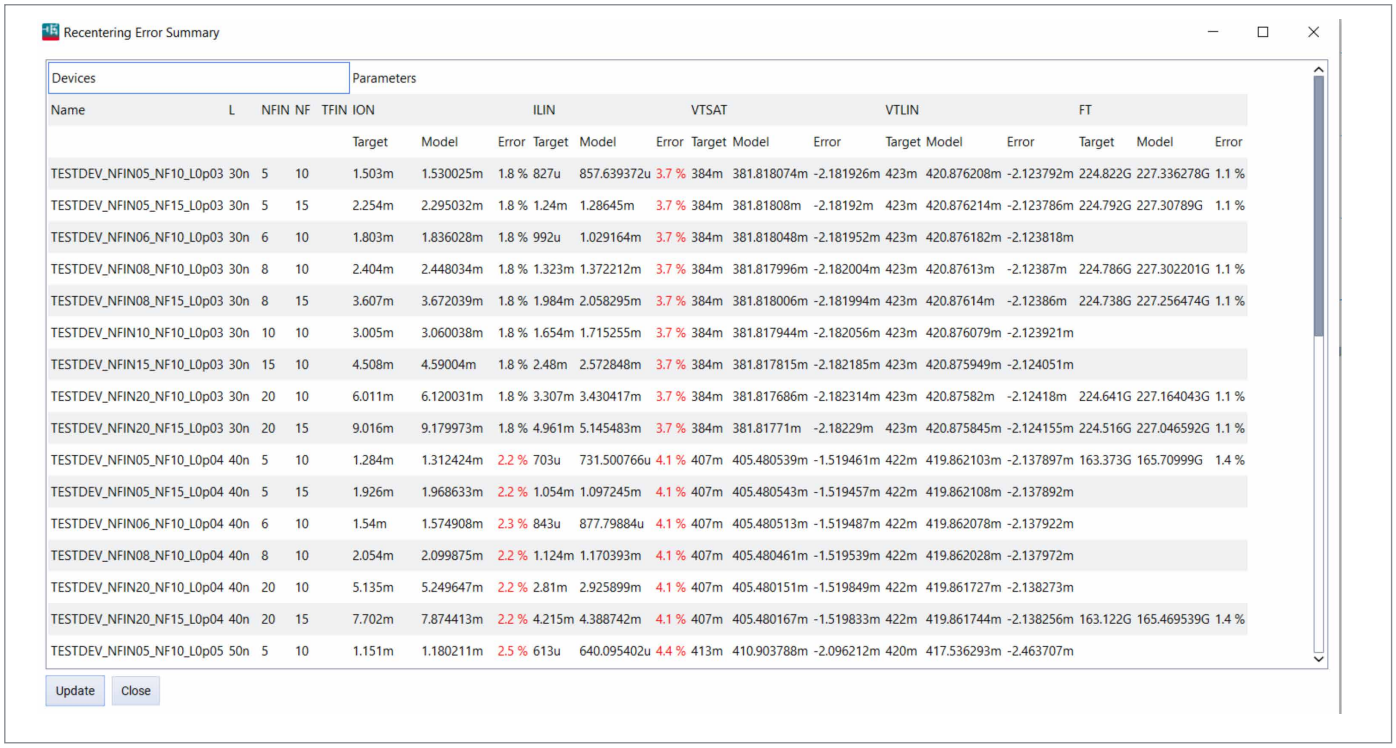


Figure 8. The recentering plots with corners turned on.

Error Summary

The Recentering Tool in the IC-CAP Model Generator also provides the Error Summary Table, as shown in Figure 9. The table displays the error between measurement and simulation for each FOM imported from the spreadsheet.

The equation used to calculate the error and the limit of the error were also imported from the spreadsheet. During Tuning or Optimization, the error coefficients are not updated in real-time to maintain tuning performance. Therefore, you need to press the Update button to re-simulate all targets for all devices in order to refresh the error calculation in the table.



Name	L	NFIN	NF	TFIN	ION			ILIN			VTSAT			VTLIN			FT		
					Target	Model	Error	Target	Model	Error	Target	Model	Error	Target	Model	Error	Target	Model	Error
TESTDEV_NFIN05_NF10_L0p03	30n	5	10		1.503m	1.530025m	1.8 %	827u	857.639372u	3.7 %	384m	381.818074m	-2.181926m	423m	420.876208m	-2.123792m	224.822G	227.336278G	1.1 %
TESTDEV_NFIN05_NF15_L0p03	30n	5	15		2.254m	2.295032m	1.8 %	1.24m	1.28645m	3.7 %	384m	381.81808m	-2.18192m	423m	420.876214m	-2.123786m	224.792G	227.30789G	1.1 %
TESTDEV_NFIN06_NF10_L0p03	30n	6	10		1.803m	1.836028m	1.8 %	992u	1.029164m	3.7 %	384m	381.818048m	-2.181952m	423m	420.876182m	-2.123818m			
TESTDEV_NFIN08_NF10_L0p03	30n	8	10		2.404m	2.448034m	1.8 %	1.323m	1.372212m	3.7 %	384m	381.817996m	-2.182004m	423m	420.87613m	-2.12387m	224.786G	227.302201G	1.1 %
TESTDEV_NFIN08_NF15_L0p03	30n	8	15		3.607m	3.672039m	1.8 %	1.984m	2.058295m	3.7 %	384m	381.818006m	-2.181994m	423m	420.87614m	-2.12386m	224.738G	227.256474G	1.1 %
TESTDEV_NFIN10_NF10_L0p03	30n	10	10		3.005m	3.060038m	1.8 %	1.654m	1.715255m	3.7 %	384m	381.817944m	-2.182056m	423m	420.876079m	-2.123921m			
TESTDEV_NFIN15_NF10_L0p03	30n	15	10		4.508m	4.59004m	1.8 %	2.48m	2.572848m	3.7 %	384m	381.817815m	-2.182185m	423m	420.875949m	-2.124051m			
TESTDEV_NFIN20_NF10_L0p03	30n	20	10		6.011m	6.120031m	1.8 %	3.307m	3.430417m	3.7 %	384m	381.817686m	-2.182314m	423m	420.87582m	-2.12418m	224.641G	227.164043G	1.1 %
TESTDEV_NFIN20_NF15_L0p03	30n	20	15		9.016m	9.179973m	1.8 %	4.961m	5.145483m	3.7 %	384m	381.81771m	-2.18229m	423m	420.875845m	-2.124155m	224.516G	227.046592G	1.1 %
TESTDEV_NFIN05_NF10_L0p04	40n	5	10		1.284m	1.312424m	2.2 %	703u	731.500766u	4.1 %	407m	405.480539m	-1.519461m	422m	419.862103m	-2.137897m	163.373G	165.70999G	1.4 %
TESTDEV_NFIN05_NF15_L0p04	40n	5	15		1.926m	1.968633m	2.2 %	1.054m	1.097245m	4.1 %	407m	405.480543m	-1.519457m	422m	419.862108m	-2.137892m			
TESTDEV_NFIN06_NF10_L0p04	40n	6	10		1.54m	1.574908m	2.3 %	843u	877.79884u	4.1 %	407m	405.480513m	-1.519487m	422m	419.862078m	-2.137922m			
TESTDEV_NFIN08_NF10_L0p04	40n	8	10		2.054m	2.099875m	2.2 %	1.124m	1.170393m	4.1 %	407m	405.480461m	-1.519539m	422m	419.862028m	-2.137972m			
TESTDEV_NFIN20_NF10_L0p04	40n	20	10		5.135m	5.249647m	2.2 %	2.81m	2.925899m	4.1 %	407m	405.480151m	-1.519849m	422m	419.861727m	-2.138273m			
TESTDEV_NFIN20_NF15_L0p04	40n	20	15		7.702m	7.874413m	2.2 %	4.215m	4.388742m	4.1 %	407m	405.480167m	-1.519833m	422m	419.861744m	-2.138256m	163.122G	165.469539G	1.4 %
TESTDEV_NFIN05_NF10_L0p05	50n	5	10		1.151m	1.180211m	2.5 %	613u	640.095402u	4.4 %	413m	410.903788m	-2.096212m	420m	417.536293m	-2.463707m			

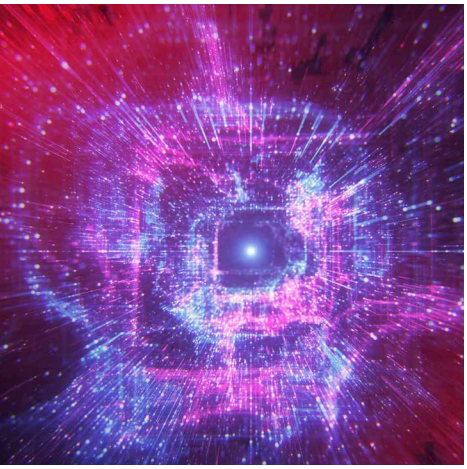
Figure 9. Recentering Error Summary table displays the error between measured and simulated for each FOM imported from the spreadsheet.

Target Modeling

Target Modeling is performed by starting from an empty project, and instead of performing Autocreate & Load on the Measure page, the targets spreadsheet is directly imported. Once the import is done, open the Scaling Plots dialog and create scaling plots. The procedure is similar to the one described above. Once the desired scaling plots are created, these plots can be used in Task > Step to do the parameter extraction.

Conclusion

The IC-CAP Model Generator Recentering Tool allows device modeling engineers to recenter an existing model based on Figures-of-Merit (FOM) targets. It is possible to apply model recentering to an existing Model Generator project in which the model was extracted using IV, CV, or S-parameter measurements. This can also be done when only targets are available. The process of recentering models can be easily implemented by creating and importing a corresponding spreadsheet. Additionally, recentering enables the user to turn on corner simulations and view the simulated corner traces, along with the typical or nominal curve being tuned or optimized.



Keysight EDA Elevates Design Intelligence at DAC 2024

These pages offer a pictorial account of Keysight's successful participation at this year's DAC – The Chips to Systems Conference 2024 held in San Francisco in late June. We sponsored the I Love DAC free exhibit pass, featured 17 customer and partner presentations in our booth theater, delivered a visionary executive SkyTalk in the DAC Pavilion, participated on an executive EDA business panel, presented several poster sessions, held numerous customer and partner meetings, entertained more than 1200 visitors in our booth theater, and hosted a very popular customer appreciation event at The Press Club.

You can relive part of our DAC experience by watching the theater presentation videos.

Watch Theater Presentation Videos

Hanging banner expressing our show theme about helping designers work smarter and more productively with new AI/ML, Python workflow automation, and engineering lifecycle management capabilities in the Keysight EDA product line.

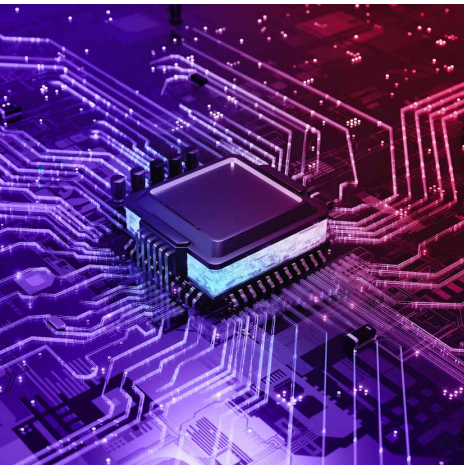
Part of the Keysight EDA crew in our beautiful DAC booth.

Can you escape from a straight jacket and ride a unicycle at the same time? Now that's entertaining!

A full house for the EDA business executive panel session moderated by Jay Vleeschhouwer of Griffin Securities with Keysight EDA VP & GM Niels Faché in the middle of the action.

Our main theater entertainers packing the booth and educating audiences about the advantages of Keysight's EDA solutions.

AWS' Ravi Poddar and Keysight's Nupur Bhonge present on hybrid cloud architectures in the booth theater.



How to Overcome the Unique Challenges in Chiplet Systems

Chiplet design represents a new era in the semiconductor design process, promising enhanced performance, cost efficiency, and scalability. However, this innovative approach also brings unique system-level verification challenges that necessitate standards for reliable operation and future compatibility.

This article covers:

- Understanding unique challenges in the chiplet design approach
- Following the Universal Chiplet Interconnect Express (UCIe) standard
- Leveraging Electronic Design Automation (EDA) tools to overcome these chiplet system analysis challenges.

Challenges in Chiplet Systems

Figure 1 shows how chiplet system design breaks different functions into smaller, separate dies, improving cost efficiency, yield, and scalability. Although the chiplet's modular approach has benefits, the functional blocks are now on different dies. This introduces:

- Increased design complexity in chiplet die-to-die (D2D) communication
- Increased verification complexity in end-to-end system performance

Consequently, a robust system-level analysis of the chiplet design is crucial in establishing reliability before production.

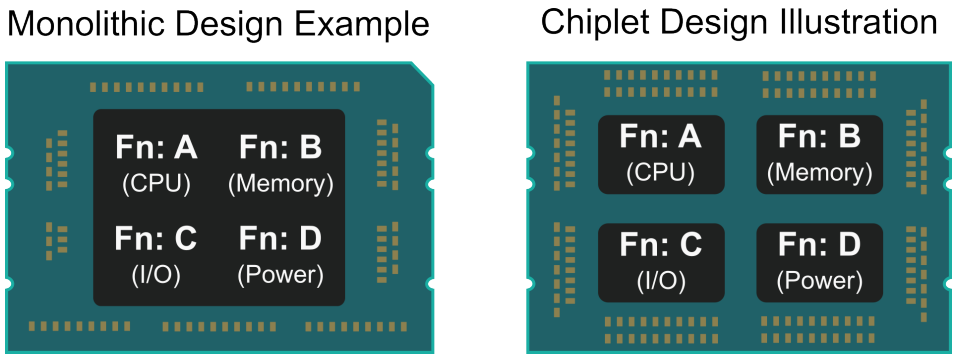


Figure 1. Comparison between the monolithic chip design and chiplet design approach. Chiplet designs have smaller die sizes to increase cost efficiency, yield, and scalability.

UCIe Standard's Guidance for Chiplet Electrical Layer

Researchers and engineers have recognized the challenges in chiplet D2D interconnect and have created standards to guide the industry. One such standard is the Universal Chiplet Interconnect Express (UCIe).

The UCIe standard defines operating data rates for chiplet systems (4, 8, 12, 16, and 32 GT/s) and sets physical dimensions and signal integrity (SI) specifications for chiplet designs [1]. The key SI metrics from the UCIe standard are:

- Eye mask
- Voltage transfer function (VTF) loss
- VTF crosstalk

The above metrics have different values depending on the data rates of the chiplet system.

As an example, Figure 2 shows the VTF loss metric. The UCIe standard provides a formula to calculate the VTF loss data line and the mask that helps determine whether the current interconnect is too lossy. To pass, the VTF loss line of your data line needs to be above the UCIe VTF loss mask.

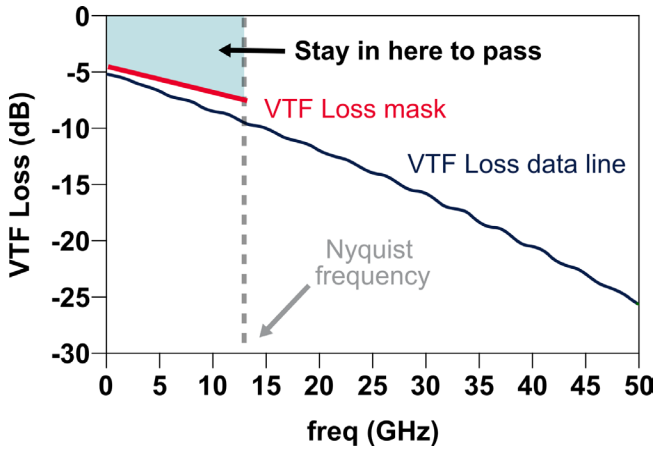


Figure 2. The UCIe standard provides VTF loss metrics for different data rates and packaging types. To pass the VTF loss metric, the VTF loss curve has to stay above the VTF loss mask specified for the given data rate and packaging type

Chiplet System Analysis with EDA

To address the unique system verification challenge in chiplets, it is imperative to utilize EDA software that offers comprehensive analysis capabilities. Key attributes to consider in an EDA solution include:

- Standards Focused: Ensure the software supports chiplet interface standards, facilitating interoperability and compatibility.
- Complete System Analysis: Look for software that offers robust end-to-end system analysis from transmitter to receiver, enabling early identification and resolution of any link issues.
- Usability and Integration: Select user-friendly software with a solution that integrates the analysis and verification into your design process.

By selecting the right EDA solution tailored to chiplet verification requirements, engineers can effectively address the verification challenges and unlock the full potential of chiplet-based systems.

Keysight EDA Chiplet PHY Designer

Shown in Figure 3, Chiplet PHY Designer is a part of Keysight EDA Advanced Design System (ADS). It has all the key attributes one seeks when performing chiplet system analysis.

Chiplet standard-driven

Chiplet PHY Designer focuses on the chiplet standards. The UCIe standard and its relevant data rate and package type are in a dropdown list. This makes the simulation setup very intuitive.

Complete system analysis

Chiplet PHY Designer understands the Tx and Rx IBIS-AMI (Input/Output Buffer Information Specification - Algorithmic Modeling Interface) models. Capabilities such as adding equalization, sending the forwarded clock, and setting different termination resistances are a few clicks away.

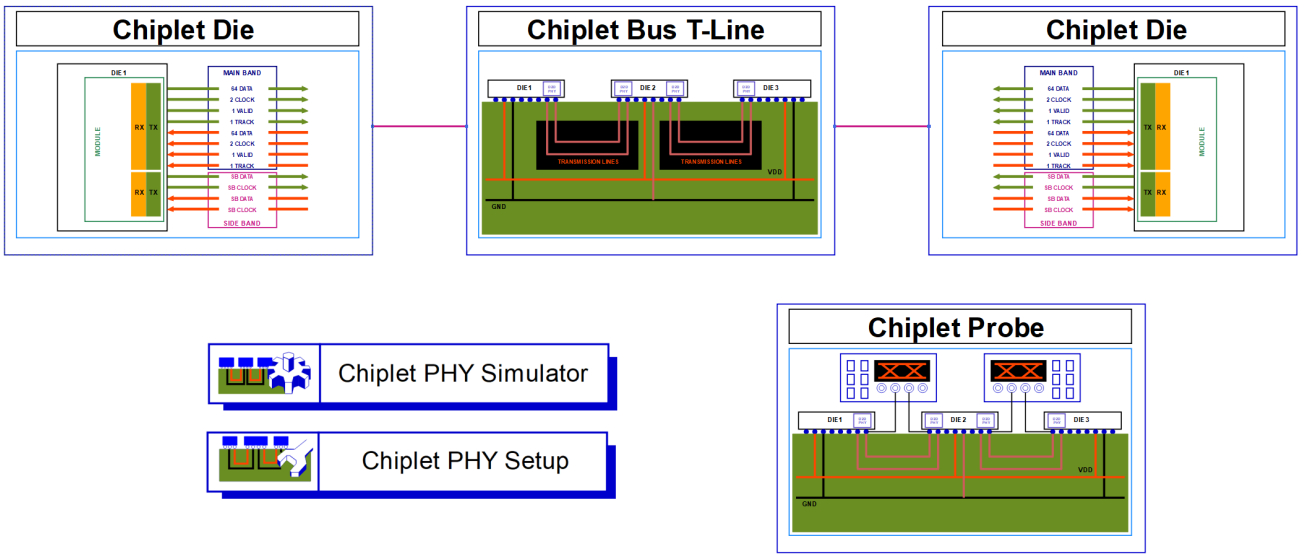


Figure 3. Keysight EDA Chiplet PHY Designer uses the block-based interface to simplify the end-to-end chiplet system verification simulation setup. It focuses on different chiplet standards, making it easy to analyze the full chiplet system.

With Chiplet PHY Designer, you can easily create IBIS-AMI models for both transmitters and receivers. You can also build a channel model using transmission lines and VIAs or import S-parameter files from a 3D Electromagnetic (EM) simulation.

Smart verification workflow

Chiplet PHY Designer includes a smart connection wizard that saves setup time by using signal names to connect 20 or more lines with just a few clicks. The design exploration feature will help you sweep through the values and generate a report for you.

Explore the Chiplet Frontier with a Good Partner

In conclusion, chiplet design represents a transformative shift in semiconductor manufacturing, offering performance, cost-efficiency, and scalability benefits. However, it also presents increased complexity in the system's design and verification.

The Universal Chiplet Interconnect Express (UCIe) standard provides essential SI specifications, addressing key issues such as VTF loss, VTF crosstalk, and eye masks for various data rates. Following the standards is crucial for maintaining a robust chiplet design.

EDA tools are essential for identifying potential system performance issues. Keysight's Chiplet PHY Designer, within the Advanced Design System (ADS), is an effective EDA solution. It offers a standard-driven approach, thorough system analysis, and a user-friendly interface. This tool simplifies the system analysis simulation setup, helping you achieve performance goals fast.

Reference

[1] "Universal Chiplet Interconnect Express (UCIe) Specification," July 10, 2023, Revision 1.1, Version 1.0.

Evolving Trends in RF and Microwave EDA

AI has contributed to the need for high-throughput, high bandwidth data transmission through wired and wireless channels. This necessitates wireless frequencies to increase upwards to the sub-terahertz (~250GHz) region to transport these massive amounts of data for machine-learning (ML) applications such as: self-driving EVs; automated mining and farming; autonomous port and warehouse cargo handling; remote surgery and healthcare; and complex dynamic defense-aerospace scenario management.

These changes impact radio frequency and microwave (RF/uW) design methodology in the following ways:

- 3D Heterogeneous Integration (3DHI) with advanced packaging techniques to combine dissimilar materials, devices, and circuits into a single module to deliver maximum functionality and performance reliably and competitively.

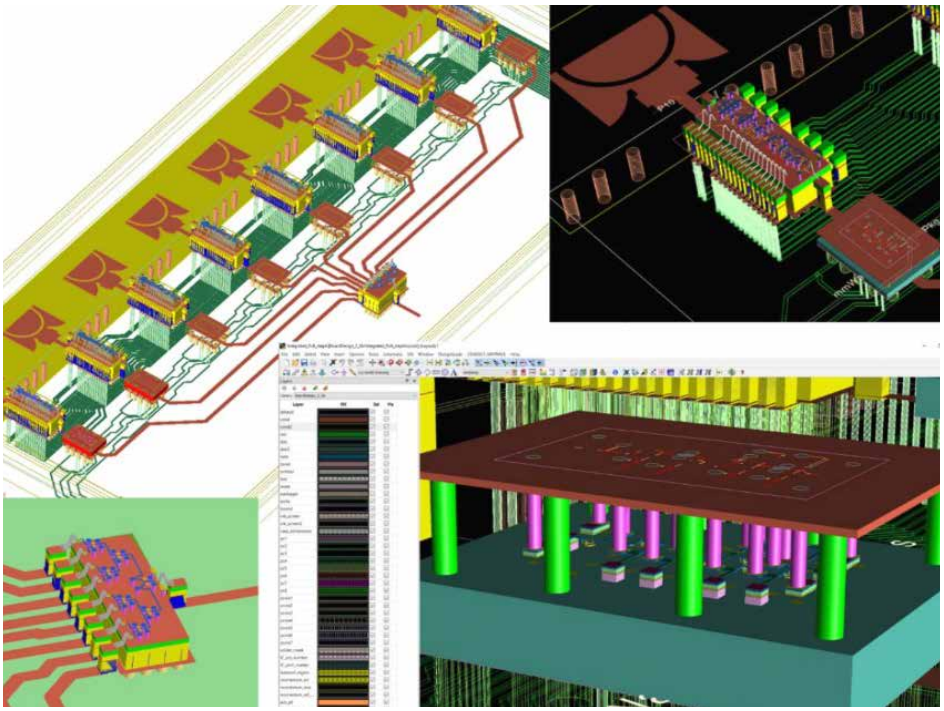


Figure 1. 3D Heterogeneous Integration of dissimilar materials, devices and circuits into single RF/uW and mmWave module that combines RFICs, MMICs, laminates, interconnects and antennas enable maximum functionality and performance with drop-in convenience for applications such as 5G, 6G and automotive radars.

Since 3DHI integrates multiple types of technologies (Si RFICs, GaN/GaAs/SiGe MMICs, laminates, interconnects, and antennas), the RF/uW component designer must now need to:

- Assemble and edit mixed technology physical layouts in 3D with stacked, flipped, adjacent, and edge placements of components.
- Correctly route 3D interconnects for RF, bias, and control signal paths between components.
- Manage multiple technology and material stackup definitions needed for accurate EM-circuit and electrothermal (ETH) simulation of RF paths through the 3DHI module. That is why Keysight SmartMount in ADS was developed to tackle the above challenging tasks.
- Verify 3D physical design across different technologies boundaries within the entire module level for LVS, DRC, ERC, and LVL compliance before simulation and fabrication.
- Simulate, troubleshoot, tune, and optimize critical RF paths through the 3DHI module- from external connectors to integrated antennas with EM-circuit cosimulation.

• Multi-physics EM-Circuit-Electrothermal Simulation access during interactive RF design

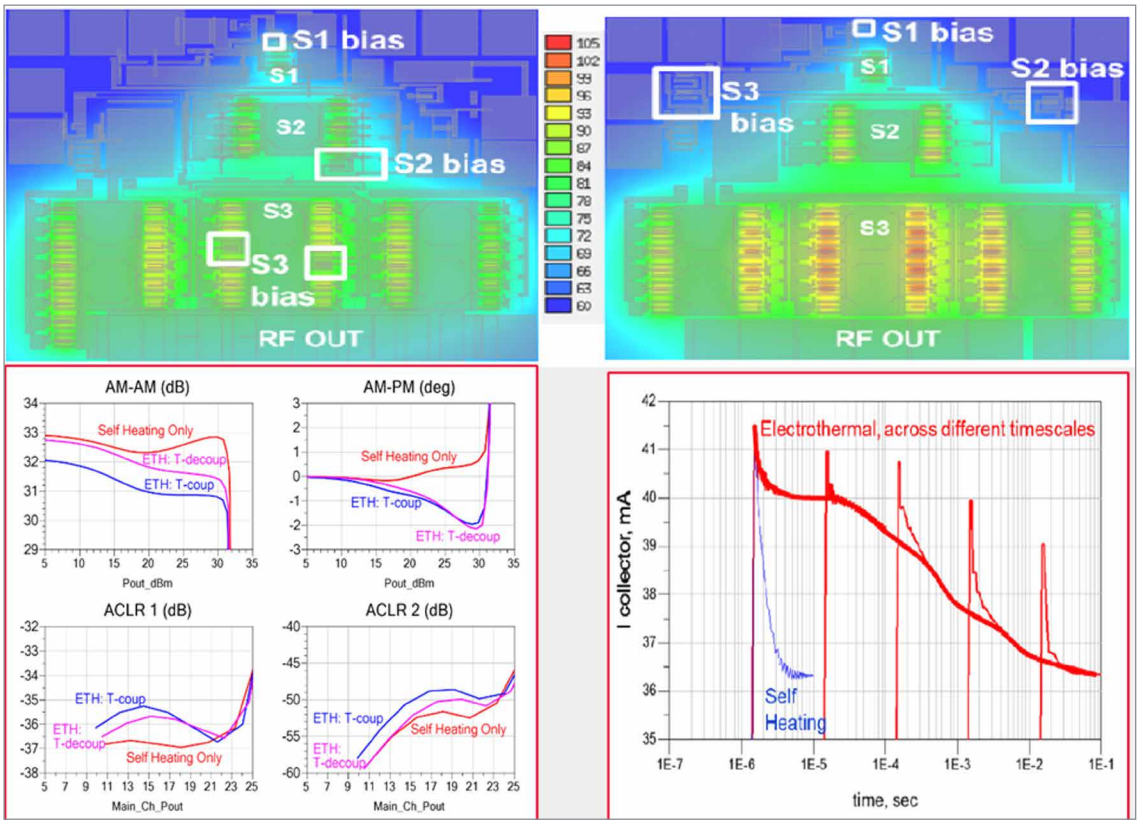


Figure 2. Electrothermal (ETH) analysis involves closed loop integration of thermal physics and circuit simulation to accurately predict steady state and dynamic localized temperature rise that alters the electrical characteristics of active devices. ETH self-heating contributes to costly failures of RF module performance and reliability, while deployed in the field for mission critical applications.

- RF critical paths traversing across multiple technology boundaries in 3DHI structures require both EM and Circuit simulation to be simultaneously used in EM-circuit cosimulation to accurately predict the physical impact of tightly integrated materials on RF performance. Keysight RFPro was developed specifically for automating EM-circuit simulation of any selected 3D layout structures by eliminating tedious traditional layout cookie cutting and manual reconnection of circuit nodes to EM ports.
- Active devices such as power amplifier (PA) and high-power RF paths in tightly integrated 3DHI structures cause steady-state and transient temperature changes during operation, which degrades RF performance during actual field deployment if not accounted for during design. Examples include PA device impedance and characteristics shifts from electrothermal heating, causing unacceptable degradation to gain, ACPR and EVM specs. This is where Keysight Electrothermal Simulation is employed together with circuit simulation to account for such effects during design to prevent costly failures in actual mission critical field deployment like satellites and self-driving EVs.

• Multi-domain (Time-Frequency-Envelope-Numeric, Linear-Nonlinear Stability, Statistical) EM-Circuit-System Simulation for thorough characterization of 3DHI modules in active operation with high data rate, digitally modulated sub-terahertz mmWave signals in densely integrated packaging.

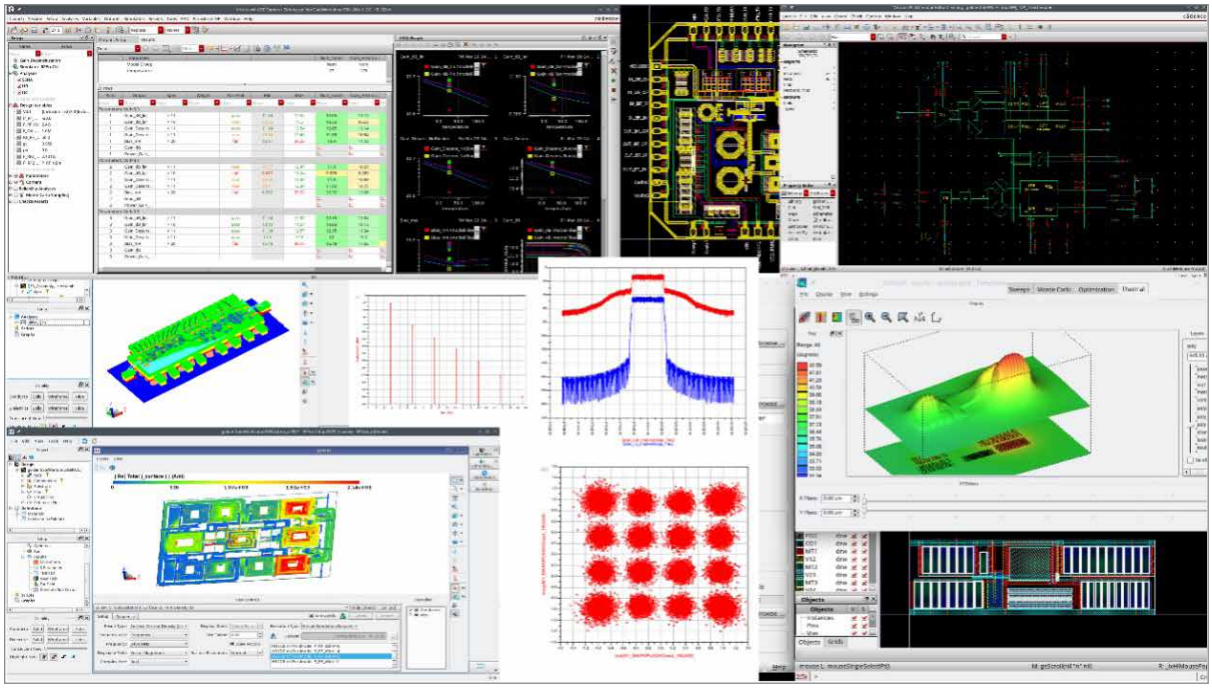


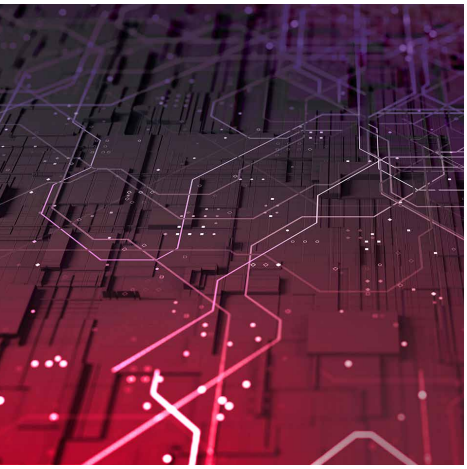
Figure 3. The next generation of RF/uW and mmWave EDA enables intuitive simultaneous access to multi-physics & multi-domain simulation to accurately design complex 3DHI modules to satisfy non-traditional Figures of Merit (FOMs) such as Error Vector Magnitude (EVM), ETH performance during field deployment, and verification of circuits to meet system specs for 5G/6G and other high bandwidth applications.

- High data rate wireless transmission requires RF designs to meet non-traditional digitally modulated RF Figures of Merit (FOMs), namely Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR).
- Accurate and fast simulation of these FOMs require multi-domain time-frequency-envelope analysis with spectrally and statistically accurate stimulus signals and instrument grade data post processing for tuning and optimization during design.
- Keysight EDA uses the same signal generation (e.g., Compact Test Signals) and data post processing algorithms (e.g., Distortion EVM) as in Keysight instrumentations for the highest simulation accuracy, and confidence in verifying simulated and measured FOMs.
- High gain PA in densely integrated 3DHI modules can suffer from unintended feedback and consequent deleterious oscillations. Keysight's Winslow linear/nonlinear stability analysis dramatically simplifies the PA circuit stability analysis setup by replacing 14 separate traditional analyses with just 1 simulation and still thoroughly output their collective stability insights.
- Circuit excitation in EM analysis of 3DHI structures surrounding the unstable PA is a valuable technique to pinpoint the physical locations and frequencies at which undesired feedback occur that cause instability. ADS Winslow nonlinear stability analysis enables PA designers to judiciously incorporate shields, absorbers and layout rerouting to guarantee stability for their intended applications.
- To compete for early design wins of your 3DHI RF modules with potential clients, Keysight's Virtual Test Benches (VTBs) incorporate industry standards such as 5G, pre-6G, and automotive radars to let you prove your design's compliance with these standards even before the hardware is finalized.

Summary

- Re-evaluate your RF/uW design workflow to prepare for AI fueled demand for wideband, sub-terahertz 3DHI mmWave circuit designs.
- Keep your business and yourself relevant with the evolution of RF/uW industry trends by deploying the prerequisite next-generation EDA technologies in your R&D workflow.
- Keysight EDA is your partner in developing the next generation of RF/uW EDA methodology for intuitive and efficient access to all simulation technologies to optimize your design workflow.

Visit our web site to learn about
RFPro Electromagnetic Simulation



Generating a Dynamic Gain Model of a Power Amplifier Circuit in Advanced Design System Using DPD Explorer and System Design (SystemVue)

This How-To article serves as a guide to generating a Dynamic Gain (DG) model from a DPD Explorer simulation of a Power Amplifier (PA) schematic within Advanced Design System (ADS). The extracted DG model is then re-simulated in a System Design (SystemVue) simulation. The DG model is a modeling technique invented by Keysight (Jan Verspecht).

Dynamic Gain Model Theory

The DG model [1] was developed to address specific characteristics desired in a PA behavioral model. It represents the output envelope signal at time t_n as a mathematical function of both the input envelope signal at the same time t_n and at the past time samples t_{n-m}. The model's design ensures it is easy to extract and validate, accurately describes linear dispersion, handles high levels of compression, and effectively captures nonlinear memory effects. These features collectively make the DG model a robust tool for accurately simulating and analyzing power amplifier behavior.

Imagine the input signal as a complex envelope $s(t)$ and the output as $r(t)$. The DG model mathematically relates these signals, considering both the present and past time samples, ensuring precise modeling of amplifier behavior. The modeled $r(t)$, $r_M(t)$, is expressed as

$$r_M(t) = h(t) * \left(s(t)\, \hat{O}[s(t)]\right),$$

with $h(t)$ representing the small signal impulse response of the system and with $\hat{O}[.]$ representing a time invariant nonlinear memory operator, also called the dynamic gain operator. $\hat{O}[.]$ has the following form

$$s(t)\left(G_0(|s(t)|) + \sum_{p=1}^{P} G_p(|s(t)|)\ \widehat{M_p}[s(t)]\right),$$

with $G_p(.)$ representing the discrete set of so-called "nonlinear gain sensitivity" functions associated with the nonlinear memory operators

$\widehat{M_p}[.]$. These memory operators have rotational invariance, meaning that $\widehat{M_p}[s(t)e^{j\theta}] = \widehat{M_p}[s(t)]$. Examples of rotationally invariant operators are $s(t-k\tau)e^{-j\varphi(s(t))}$, $s^*(t-k\tau)e^{+j\varphi(s(t))}$ or $|s(t-k\tau)|^2 - |s(t)|^2$.

In practice, we add the additional constraint $\widehat{M_{p>0}}[s(t) = constant] = 0$, such that $G_0(.)$ corresponds to the static steady-state AM-AM AM-PM characteristic.

One of the most powerful uses of the DG model is Digital Pre-Distortion (DPD), where a behavioral inverse model is used to pre-distort the input waveform such that the output waveform is free of distortions.

Extract a Dynamic Gain model from a DPD Explorer in ADS simulation

Let's dive into the process of extracting the DG model. This involves identifying the nonlinear memory operators $\widehat{M_p}[.]$ and the associated gain sensitivity functions $G_p(.)$. Often, a few samples of the power difference operator effectively capture the nonlinear memory effects.

For the identification, three key data sets are needed:

1. The PA IQ input signal.
2. The PA IQ output signal.
3. The PA linear gain across a bandwidth at least as wide as the IQ signal.

These can be obtained either through measurements using a PNA-X and a vector signal generator, or from simulation, if the circuit design is available in ADS.

When the DG Model is selected as the DPD model extraction type, the DPD Explorer in ADS simulation provides these essential sets of data, along with inverse DG model file, after simulation. DPD Explorer in ADS records both the PA input and output signals, which can be found in the log folder. The path to this folder is displayed in the simulation control window. The files are:

- DPD_Iteration0_PA_Input_Real.txt
- DPD_Iteration0_PA_Input_Imag.txt
- DPD_Iteration0_PA_Output_Real.txt
- DPD_Iteration0_PA_Output_Imag.txt

The S21 data within the inverse DG model file represents the linear gain of the PA. DPD Explorer in ADS stores the inverse DG model in a csv file generated under the ADS workspace folder.

It is crucial to ensure that nonlinear dynamics are excited during this characterization. Subsequently, a realistic modulated stimulus signal—typically a periodic pseudo-random sequence that mirrors the statistics and power spectral density of the targeted modulation format—is applied.

To demonstrate the model extraction process, I used the "UsingDPDExplorer_mmWavePA_wrk.7z" installation example PA and ran a DPD Explorer in ADS simulation to obtain the inverse DG model file.

Once the DPD Explorer in ADS simulation data is available, the DG model is generated in System

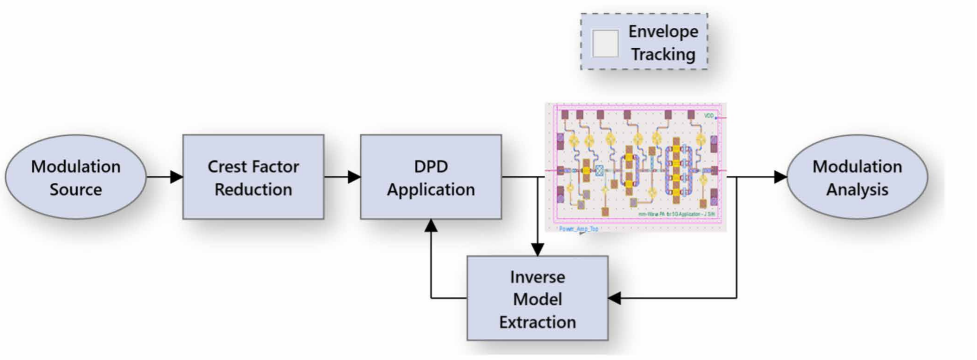


Figure 1: DPD Explorer in ADS.

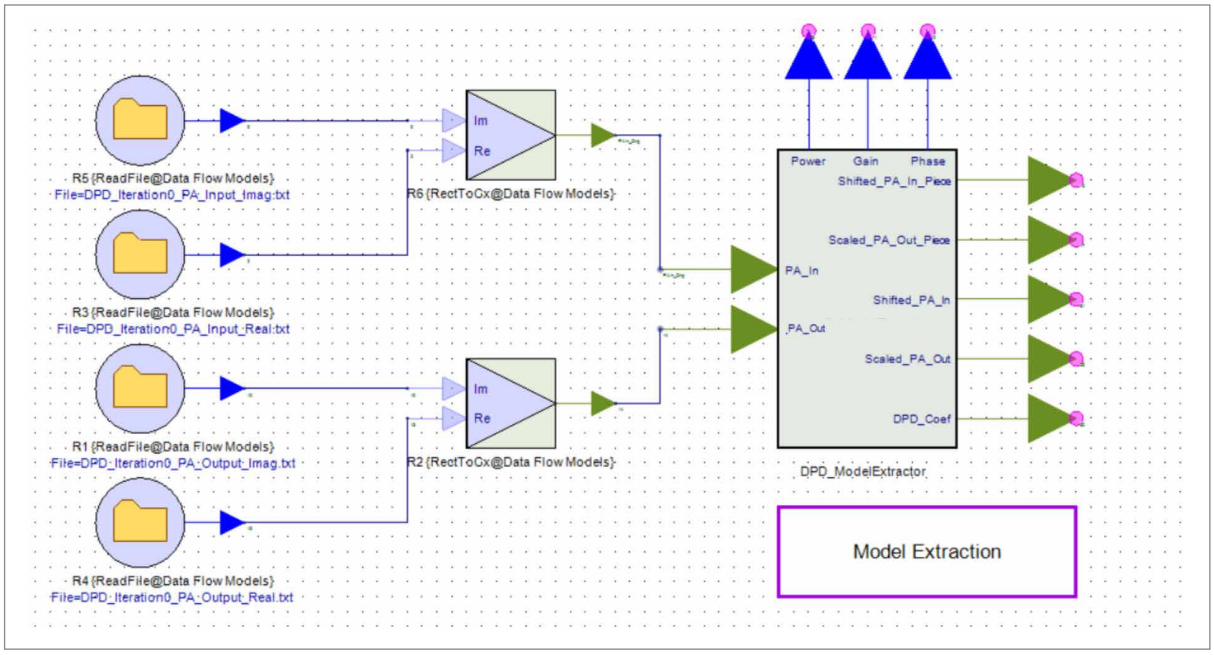


Figure 2: DG model extractor design.

Design (SystemVue) using a small variation of the "PA DPD Model Extraction.wsv" installation example. This modified example, called "PA DPD Model Extraction from ADS.wsv," produces the DG model file saved as DGPAModel.csv. This model is now ready for use in SystemVue simulations, including applications of Digital Pre-Distortion (DPD).

Simulate the Dynamic Gain model

The extracted DG model can then be re-simulated in a SystemVue simulation. The Dynamic Gain model can be read using the DPD_PreDistorter model.

The comparison between the DG model and the original circuit is shown below. The input signal is the same that was used in DPD Explorer in ADS.

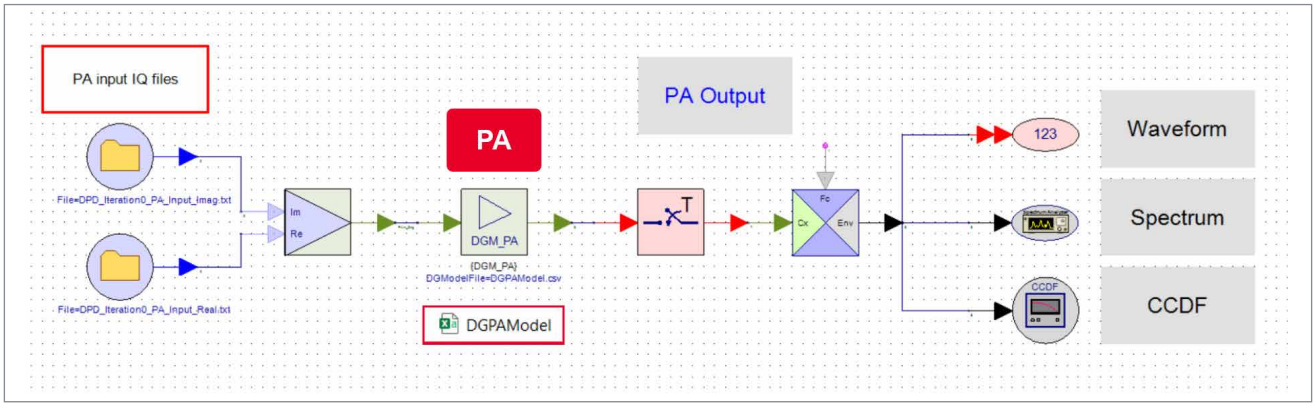
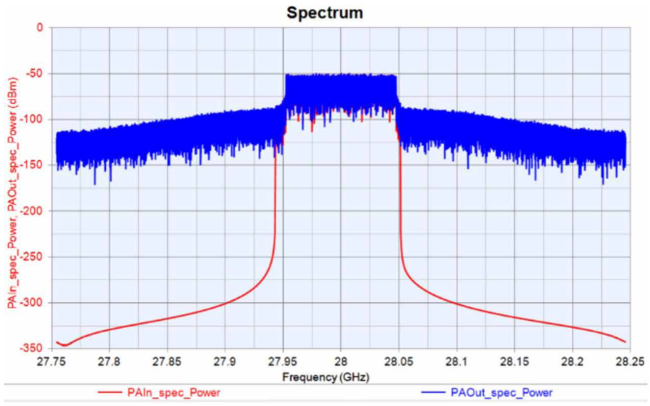


Figure 3: Design using the DG model in simulation.



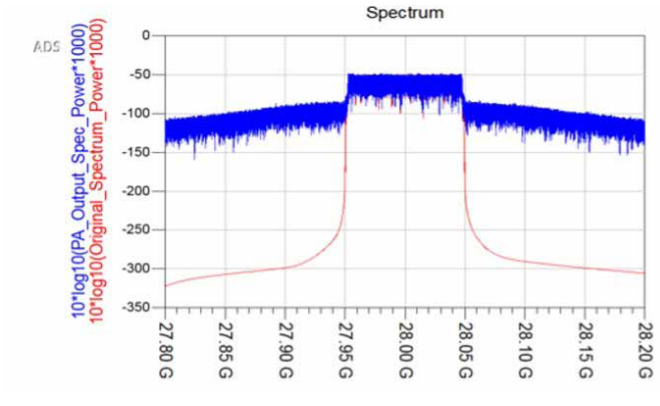


Figure 4: PA input/output spectra comparison: SystemVue (DG model) vs. ADS (circuit).

Mean Power (dBm	Peak Power (dBm)
-13.999	-6.023
21.316	28.295

Figure 5: Mean and peak PA input/output power in SystemVue with DG model.

Peak Power (dBm	Mean Power (dBm)
-6.238	-13.991
28.188	21.324

Figure 6: Mean and peak PA input/output power in ADS with PA circuit.

A very good agreement between the prediction of the model and the reference results using the actual amplifier circuit design in ADS can be observed.

Accessing Workspaces and Additional Resources

To access the workspaces mentioned in this article, you can find them on this Knowledge Center page.

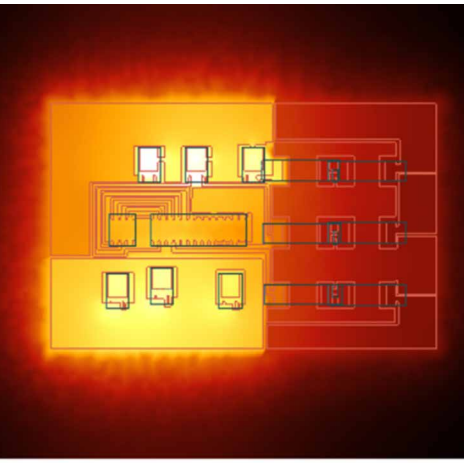
For more information about DPD Explorer or to see related videos and tutorials, please visit the Keysight DPD Explorer product page or check out our YouTube channel. This will provide you with additional resources to get the most out of your simulations.

Conclusion

With this guide, you have learned another way to leverage data generated by DPD Explorer simulations. This article has walked you through the process of generating a Dynamic Gain model using DPD Explorer in ADS and resimulating it in SystemVue. The DG model, with its ability to capture complex PA behaviors, is a powerful tool for engineers working on power amplifier designs.

For those looking to explore further, we recommend diving into the example workspaces and leveraging the resources available on Keysight's website.

Reference [1] JAN VERSPECHT, "Innovations in characterizing and modeling modulation distortion in active components", 17th European Microwave Integrated Circuits Conference, Mila, September 2022.



Power Converter Design in the Age of Wide Bandgap Semiconductors

The rise of wide bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) devices is driving the next generation of power electronics technology. Wide bandgap semiconductors allow for greater power efficiency, smaller size, lighter weight, and eventually lower overall cost in the electronic devices that run our world. They enable power converters such as switched-mode power supplies (SMPS) to operate at higher switching speeds which in turn allows magnetics and capacitors to be smaller and lighter. However, these higher switching speeds also bring about new design and simulation challenges.

Higher switching speeds can generate large voltage spikes due to parasitic inductance in the printed circuit board (PCB) layout, especially in the presence of high di/dt values. Higher switching speed can also generate unwanted conducted and radiated electromagnetic interference (EMI). When unaccounted for these factors often cause the SMPS design to fail. To overcome these challenges, designers need to rethink their existing design workflow.

In a traditional design workflow for power converters, there is very little simulation followed by a long series of prototype and debug cycles, which takes a huge amount of time. With emerging wide bandgap technology, designers must find a way to identify problems in the design phase before the first prototype is produced. This not only saves money, but also speeds up the entire development process and accelerates time to market. That is the goal of Keysight ADS and PEPro (Figure 1) – the bundled simulation environment that includes models, electromagnetics and circuit co-simulation, and several other tools specifically developed to accelerate the power electronics engineering workflow.

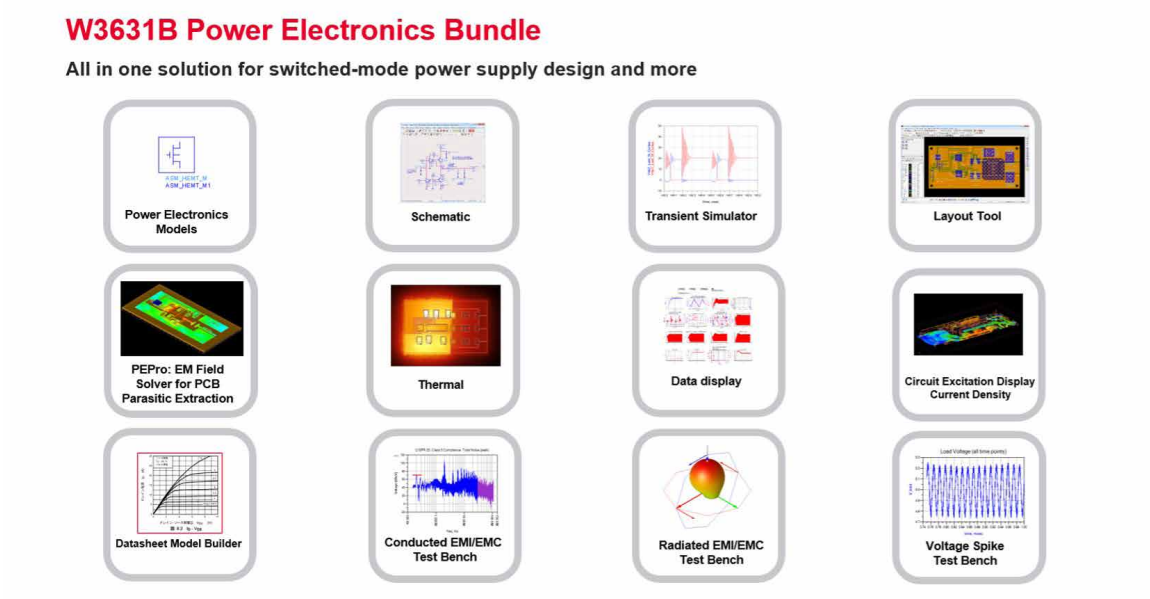


Figure 1: Power electronics design and analysis bundle.

There is a steady state solver (Shooting Newton) for precise analysis of periodic steady-state signals and closed-loop analysis. It also offers transient design simulation for deep insight into switching characteristics, including open-loop analysis, and an electromagnetic solver for simulating the effects of PCB layout parasitics. Unlike traditional SPICE circuit simulation, ADS integrates a field solver with the SPICE-like circuit solver, linking distributed elements in the layout with lumped elements in the schematic. The simulation runs in two stages. First, the field solver extracts an EM-based model of layout parasitics. In the second stage, the EM-based model is added to the transient (SPICE-like) circuit simulation. An example of this is shown in Figure 2.

The simulation produces extensive data, viewable in ADS's powerful data display and 3D viewer. The EM-model informs circuit simulation, identifying issues such as voltage spikes or ringing, which can be confirmed by measurement. Circuit waveforms also inform the EM post-simulation visualization display, revealing current crowding and hot spots.

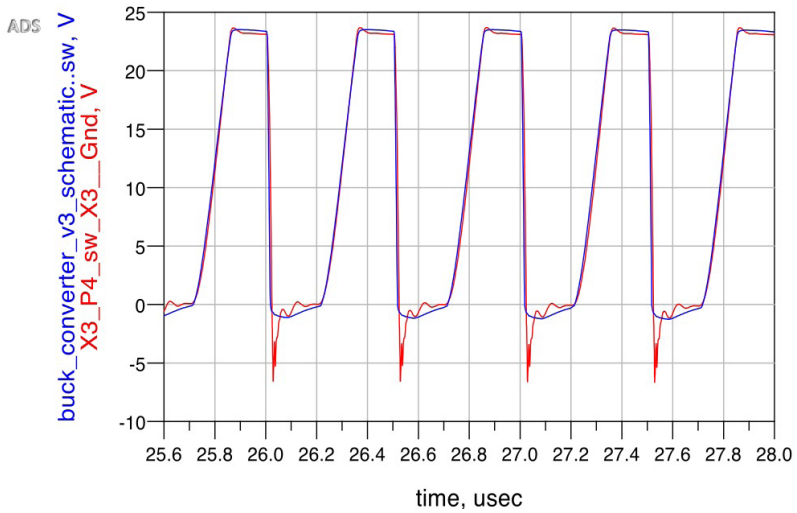


Figure 2: Buck converter steady-state transient simulation.

Blue: Ideal switching signal of a buck converter with lumped-element circuit.

Red: Switching signal of buck converter including parasitic effects from EM extraction.

A common failure mode in power supplies is localized heating due to excessive current density. Inner layer near-field visualization enables crucial examination of currents and fields for long-term reliability. By using multiple sources of field data and excitation, an entire power supply can be accurately characterized along with the PCB layout to find and fix current density and EMI problems before expensive prototyping even begins. Figure 3 is an example of current density in the PCB layout of a SMPS.

Current Density is just half of the picture. High di/dt currents in the design can lead to unwanted EM radiation and I^2R losses that make hot spots. As such, a comprehensive virtual twin of a power supply design must have electromagnetic models including EMI (radiated and conducted), as well as thermal analysis. The PEPro bundle includes these capabilities, with thermal modeling as the newest addition to the workflow. As shown in Figure 4, thermal analysis can be performed at the semiconductor and schematic level to estimate operating temperatures, and then incorporate PCB layout and ambient conditions for highly accurate results.

Request a Trial

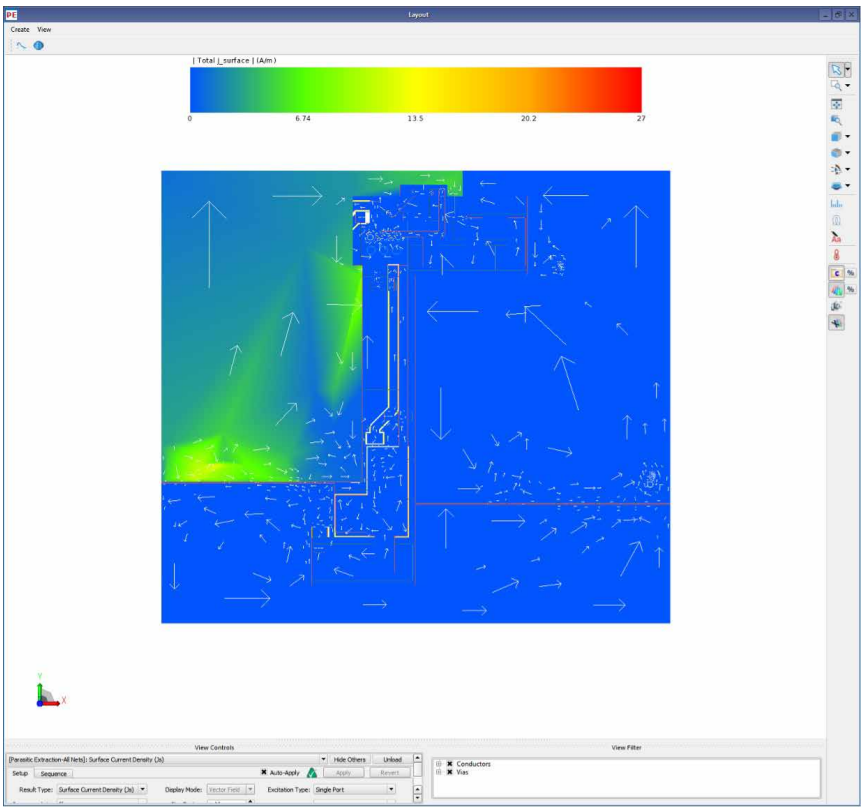


Figure 3: Current Density in a SMPS PCB Layout.

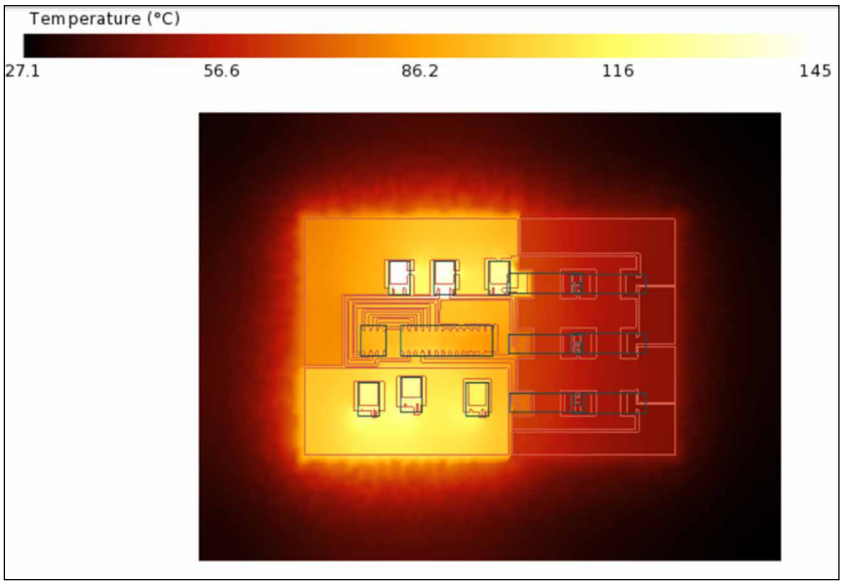
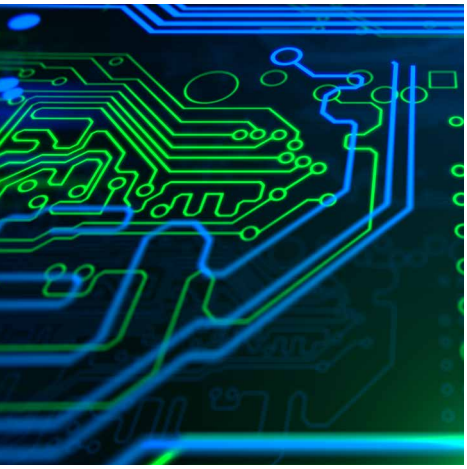


Figure 4: Thermal analysis heatmap visualization of a 3-phase DC-AC inverter PCB.



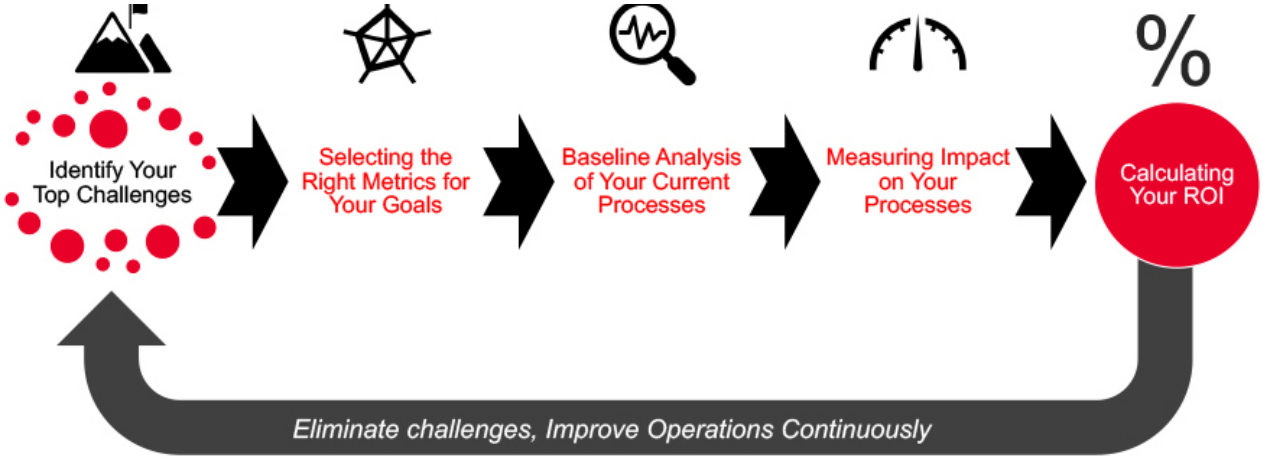
The ROI Equation: Mastering Success in IP-Driven Semiconductor Design

Return on Investment (ROI) is a universal metric used to assess the profitability of an investment. It is easily understood in casual conversations across all industries. It is a straightforward and effective tool for determining the profitability of tools and processes, making it easy to communicate and compare investments universally. However, Calculating ROI in semiconductor IC design, particularly in Intellectual Property (IP) development methodologies, presents a unique and intellectually stimulating challenge. It's more than a simple matter of plugging numbers into a formula. It demands a profound understanding of the intricacies of IC design and the specific nuances of IP development.

While many semiconductor design teams effectively use IP development methodologies, calculating the ROI for their IP processes is a rarity. This is due to the following reasons, as stated by IC design managers:

- **Challenges in Quantifying Benefits:** Many benefits of IP reuse are intangible and difficult to quantify financially. For example, faster time-to-market due to using pre-designed blocks is valuable, but assigning a specific dollar value to it can be tricky. Other intangible benefits include improved product quality, enhanced customer satisfaction, and increased market share.
- **Long-Term Impact:** The true value of an IP block might only be realized for some projects or chip designs down the line. Calculating ROI often focuses on short-term returns, which might not capture the long-term benefits of a well-designed IP library.
- **Indirect Cost Allocation:** The costs associated with developing and maintaining IP libraries are often indirect and spread across multiple projects. This concept, known as indirect cost allocation, refers to assigning a portion of these shared costs to each project. Accurately isolating the specific expenses of IP processes for ROI calculations can be challenging.
- **Focus on Functionality:** The primary focus in IC design is often on functionality and meeting design goals. While IP reuse can save time and resources, calculating the exact ROI might only be essential for some projects.
- **Industry Standard:** No well-established standard formula for calculating ROI specifically for IP management in IC design.

While calculating a precise ROI for IP processes might be challenging, companies must recognize the significant benefits of IP reuse as shown in this figure. This understanding can profoundly impact their operations, improving efficiency, reducing costs, and enhancing product quality. IC design managers across diverse industries have identified three key ROI benefits from IP adoption. First, pre-designed and verified IP blocks drastically accelerate design cycles, reducing time-to-market. Second, the use of well-tested and documented IP significantly enhances product quality by minimizing errors. Lastly, effective IP traceability streamlines compliance with industry standards like ISO 26262, ensuring seamless project management and accurate documentation. These advantages consistently emerge as top priorities for organizations seeking to optimize their IC design processes.



This figure shows a process for calculating the ROI of IP Management. Admittedly, this is an oversimplification of the actual procedure almost any organization will follow because of the reasons we identified earlier by some of the thought leaders in IC design development. For that reason, each organization must look to develop its IP management calculator. Consequently, the process will be different for each organization while primarily following the guidelines in the above figure.

Technology and business models are paramount for semiconductor design businesses—from IC manufacturers to niche vendors. IP management ROI varies widely and requires a tailored approach. Building a custom ROI calculator offers several advantages:

1. Customized ROI calculators align with unique business strategies and market conditions.
2. Bespoke tools address specific challenges and internal processes for accurate assessment.
3. Developing an in-house calculator fosters ownership, accountability, and continuous improvement.

In essence, developing a customized IP management ROI calculator empowers organizations to take control of their intellectual assets, aligning their measurement frameworks with strategic objectives, industry dynamics, and internal realities. By embarking on this customization journey, organizations can unlock the actual value of their intellectual property and chart a course toward sustained competitive advantage and innovation excellence.

To assist engineers and managers in adopting a more organized approach to intellectual property (IP) management, Keysight Technologies has authored a white paper on How to Calculate the ROI of Semiconductor IP Management. We explore the significance of categorizing IPs based on development methodology -to reveal valuable insights into the return on investment (ROI) in IP management. Despite abundant real-life examples, this white paper focuses on three case studies. While maintaining the confidentiality and secrecy of the respective business entities involved, each case study exemplifies the thought leadership of some unnamed heroes in formalizing ROI calculations for IP management.

An IP management platform is crucial in measuring ROI for IP management by providing a centralized and streamlined mechanism for tracking, analyzing, and optimizing intellectual property assets. Keysight IP Management Platform (HUB) is a powerful tool for implementing their IP management strategy and measuring ROI. HUB provides comprehensive centralized IP data management, collaboration capabilities, and traceability features that can be integrated non-intrusively into existing EDA tools and flows. By leveraging a rich set of integration capabilities, organizations can optimize the value of their intellectual property assets and drive greater returns on their investment in IP management with the guidance and support of Keysight's seasoned experts.

Unlock your semiconductor design potential today. Discover the customized approach to IP management success with Keysight IP Management Software. You can tune your ROI Recipe for Semiconductor IP management and take your innovation to the next level. Download the white-paper and learn more.

Companies like Allegro Micro have already realized the benefits of implementing an IP management strategy. By streamlining their IP management processes, Allegro saved up to 50% in design time. To learn more about how Allegro achieved these impressive results, check out Allegro Micro's case study and watch the video.

Accelerate your Digital Transformation with ADS Python Automation

The ADS 2025 software release greatly expands the Python APIs, enabling three new use cases that will drive personal productivity, enable enterprise automation, and form a foundation for engaging AI/ML.

This Python expansion started with quickly evolving design requirements in the wireless, automotive, and defense industries. Exponential growth in complexity, a worldwide design talent shortage to meet time-to-market demands, and the emergence of AI and machine learning as part of the design process are all demanding new approaches and workflows.

In response, Keysight has significantly renovated the ADS platform, beginning with the ADS 2025 release. The ADS platform has become more modular and more extensive APIs have been published to take advantage of that modularity. A specific focus has been made on the Python language, in order to take advantage of macro industry trends in programming skills, SW development tools, HPC, enterprise scaling, and AI.

The 3 use cases are:

1. **Increased personal productivity** – for traditional end-users and designers
2. **Greater enterprise automation** – for EDA workflow developers and software professionals
3. **Exploring AI/ML** – enablements for Data Scientists and algorithmic researchers

Personal Productivity	Enterprise Automation	Exploring AI/ML
For End-users & Designers who need to design hardware products more efficiently	**For EDA Workflow Developers** who write software that streamlines workflows for a team	**For Data Scientists** who ransform insights with applied Machine Learning and AI
New Use Models Enabled • Menu-based Task automation • Interactive Jupyter-style command line interface • Standalone apps	**New Use Models Enabled** • Scalable verifications • Multi-tool workflows • Enterprise orchestration • Data and IP Management and Engineering Lifecycle	**New Use Models Enabled** • Trusted Training Data Generation • Multi-domain Optimization • Domain awareness for AI/ML development

Figure 1. Follow the links at the end of this article to learn more, and watch for our upcoming Launch Events.

1. Increased Personal Productivity

One advantage of Python is its easy accessibility to entry-level programmers. Python is free and widely supported on Windows and Linux, yet is expandable with plug-ins. Anyone from PA designers to dedicated software developers can learn Python quickly, and now have a variety of ways of running their code with ADS, listed below

- Add Python scripts to your ADS menus for convenience, and invoke them directly
- Run Python code and API calls interactively from the ADS Python Console using text commands. Outside ADS, do the same using Jupyter Notebooks. Either way, these text sessions are great for capturing Expert-supervised design flows that can be edited and re-executed later.
- Build a standalone application with its own GUI. Examples are shown below.

2. Enterprise Automation

Organizations with larger design teams have additional opportunities for design automation and product lifecycle management. Since Visual Studio code and Jupyter environments can directly connect to ADS sessions to do interactive debugging, software developers can take full advantage of IntelliSense and Copilot features that are already established for Python developers.

Here are some typical applications enabled by the new Python APIs in ADS 2025:

- **Smart libraries**, PDKs, and artwork/schematic generation
- **Multi-vendor workflows**, import/export, translation, and pre-processing for fabrication
- **Scalable verifications** to perform corners, statistics, Design-for-Manufacturing, nightly integrations and regression testing, achieve sign-off for requirements flows.

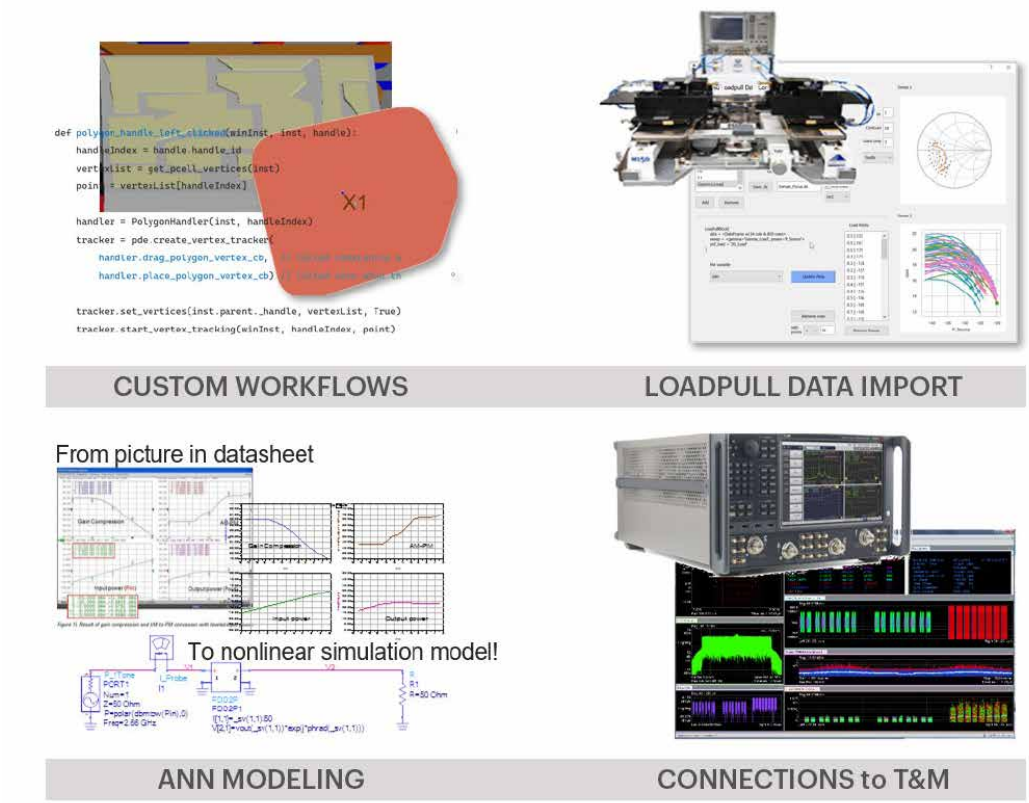
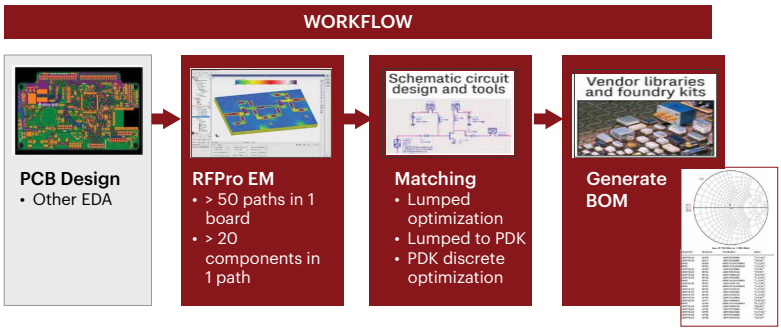


Figure 2. User-contributed Python applications both inside and outside the ADS environment.



Time per RF Path	RFPro EM, with setup	Matching Design	Bill of Materials
Traditional workflow (manual)	60 mins	40 mins	20 mins
Automated workflow	5 mins	10 mins	10 secs
Solution approach	Python for manual steps to import & prep for RFPro	Faster optimization with better initial constraints 1-button replace ideal >> vendor parts	1-button BOM generation

Results	Total Time 1 RF Path	Total Time 50 RF Paths
Traditional workflow (manual)	120 mins	6000 min (100 hrs)
Automated workflow	15 mins	750 min (12.5 hrs)
Solution approach	Improve each Task within the Workflow, using automation	

Figure 3. Automation of repetitive RFPro design and trace-checking tasks resulted in 8x speed up (note 1).

Note 1: "Accelerate RF Board BOM Simulation with ADS Design Automation", DAC 61, June 2024, https://61dac.conference-program.com/presentation/?id=ETPOST126&sess=sess232

- **Enterprise orchestration** can leverage the APIs of several databases and EDA vendor's products to perform product validation, thermal, mechanical, power, and other analyses.

3. Exploring AI/ML

- **Training Data Generation** – AI/ML algorithms are dependent on the quality and contents of the training data. Keysight simulators and measurement system provide accurate and trusted data sources. Together with PathWave Data Tools for formatting, tagging, and data reduction, ADS is a natural platform to power your AI/ML modeling and application development.
- **Multi-domain Optimization** – ADS can be controlled using its APIs to perform many types of simulations, while also making parameterized adjustments to schematics and geometric/ artwork dimensions in the physical design. This enables external optimization across multiple engineering domains relatively straightforward using PyTorch, TensorFlow, and other tools.

For More Information

Visit these links for more information about Keysight EDA's support for Python automation and AI/ML:

- ADS Python resources https://www.keysight.com/find/python-eda
- ADS AI/ML resources https://www.keysight.com/find/eda-ai-ml
- Anurag Bhargava Python tutorials - https://www.youtube.com/watch?v=ejPoR8tm7GA

One of Keysight's innovative EDA leaders is Matt Ozalas, product owner for Keysight Advanced Design System (ADS). Regarding RF design and EDA tools, SHIFT LEFT had a few questions for Matt as he recently celebrated his 10th anniversary working for Keysight.

A Few Minutes in the EDA Mind of Matt Ozalas

What are some of your career highlights?

"One highlight is traveling around the world and meeting engineers from different cultures," he says. "I realized we're all trying to solve the same problems." Matt is probably best known for his pioneering work on power amplifier stability and the WS-Probe working with Dr. Tom Winslow. "We were able to get the WS-Probe into designers' hands – it was one thing to release the technical solution, but the other thing was getting people to realize how valuable it is."

Why is your Power Amplifier video series so popular?

"Conference papers and app notes were either too advanced with new info or too vague with too many assumptions about background theory," he shares. "I chose the Power Amplifier topic because wireless technology was taking off, and only a few people knew in-depth about power amplifier design. Younger engineers were asked to work on complicated designs but never got to step back and learn the theory. I tried to create material with respect for the history of radio, with concepts from the 1930s so people would understand the basics."

What are the hot topics in RF EDA right now?

"Higher frequencies and increasing complexity are on everyone's mind right now," Matt begins. "6G takes all the challenges of 5G to another level, and it's a nightmare for engineers because designs have to meet all the criteria – many different technologies have to come together for things to work. Non-linearity, parasitics, and packaging all factor into models."

How do your efforts fit in the bigger Keysight picture?

"We're in a unique position at Keysight. Other instrument companies don't have EDA products. Other EDA companies don't build instrumentation. We do both – we call it unified measurement science – putting advanced, high-frequency technologies into instruments and EDA software." Matt points out that Keysight uses its software to develop its hardware, improving performance and reducing costs.

How are design workflows changing?

"Shift left is an interesting concept, essentially creating higher fidelity models earlier in the design process." Matt cites an example of an artificial neural network (ANN) engine in ADS that can use a picture of a graphical plot of a power amplifier measurement to create a non-linear behavioral model for simulation, and then put that model into a bigger architectural model to see how the power amplifier performs in a system.

What are your key challenges in guiding ADS development?

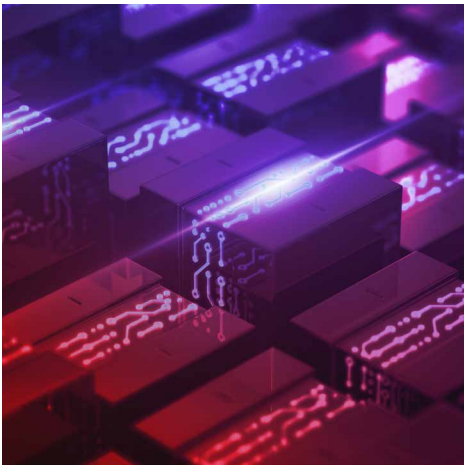
"We get a lot of requests, and there are many different ways we can solve them," Matt says. "Sometimes there is a big project like the ANN capability, but more often, it's smaller things we do every day in sprints. We constantly ask ourselves questions. Are we doing the right thing? Should we be doing something else? Are we aligned with what other R&D teams are doing? We also try to view problems and solutions from other people's perspectives."

What's the EDA market lacking right now?

"If we look at EDA tools right now, there are two different approaches. One is to collaborate, be open, and work with partners and other tools. The other is to wall off and create your own proprietary solution. However, in reality, no one vendor meets all the needs of the industry, so the way forward is more collaboration." Matt sees a similar choice ahead in AI – vendors can bury it deep inside their engine or expose it for designers to use in their workflow.

So, if you had a magic wand ...?

"This may sound ridiculous, but I'd take what we have and chop it up, kind of like Lego blocks – disaggregating bigger tools into smaller ones that designers can reassemble into their workflow. Workflows are too rigid right now. The future will be about adaptability. In 10 or 20 years, I think there will be this creative mode where people put together tools and techniques to build their things. Good things happen when we think about hardware and EDA software with that in mind.



Quick Takes

Keysight ADS Receives ISO 26262 Certification

ADS has recently achieved its ISO 26262 certification from TÜV SÜD (tool classification level 1).

Read the Story

RFIC Design with Keysight 3DEM and RF Circuit Simulators inside Synopsys Custom Compiler

Watch this partner interview and demo video from IMS 2024 where Keysight and Synopsys have integrated electromagnetic simulation directly into the Custom Compiler layout environment. See how electromagnetic effects are efficiently analyzed in a 28 GHz PA circuit with automatic EM-circuit co-simulation. Next, the power amplifier is stimulated with 5G NR modulated RF signals and analyzed for Error Vector Magnitude performance with Keysight instrument-grade algorithms for signal generation and analysis.

Watch the Video

Antenna Simulation Accuracy to Match Anechoic Chamber Measurement

Watch this partner interview and demo video from IMS 2024 that shows Keysight ADS RFPro simulating 3DEM encrypted models of Johanson Technology's off-the-shelf antennas for wearable devices. The accuracy of simulation has been verified with anechoic chamber measurements to within 5%-10%. ADS RFPro enables you to design the RF board and housing for these wearable antennas and realistically simulate and visualize the far field performance before building actual hardware. This cuts board turns from 3 to 1 and avoids wasting multiple costly anechoic chamber measurements to achieve one-pass design success.

Watch the Video

System Design Article Featured on Cover of Microwave Journal

System architects and phased array designers can download the recently published cover story entitled "Efficiently Simulating Phased Arrays with Active Impedance" from the July issue of Microwave Journal magazine.

Read the Story

Google and Keysight Joined Forces to Enhance Quantum Circuit Simulations with Frequency-Domain Flux Quantization

Check out this technical research paper about new developments in quantum circuit simulations co-authored with Google.

Read the Paper

Keysight Introduces System Designer for PCIe® and Chiplet PHY Designer for Digital Standards-Driven Simulation Workflows

Read the product introduction press release about the latest in high-speed digital standards simulation tools.

Read the Press Release

AIST Determined the Low-Frequency Noise Source in Cryogenic Operation

Japan's National Institute of Advanced Industrial Science and Technology (AIST) is using the Keysight E4727B Advanced Low-Frequency Noise Analyzer to expand the understanding of noise sources in quantum computing, paving the way for faster machines moving forward.

Read the Case Study

The Git Dilemma: Is Version Control Enough for Semiconductor Success?

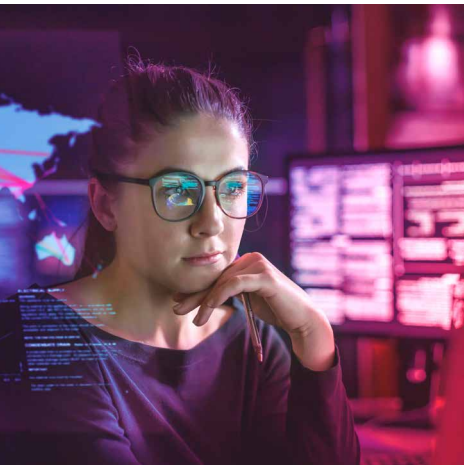
Read this blog about the pros and cons of using Git for version control on our SemiWiki channel.

Read the Blog

ESD Alliance Interviews Keysight EDA VP&GM Niels Faché

Read the blog about the career journey and management philosophy of Keysight's EDA industry thought leader.

Read the Blog



Reader Challenge

EE Fundamentals

A 100W incandescent light bulb is designed to run from a $120V_{RMS}$ AC sinewave power source at 60Hz, the standard in North America.

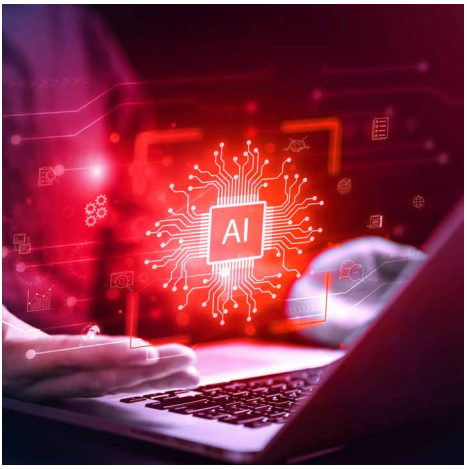
If the light bulb is lit at full rated power and operating in its steady state, how many electrons are flowing through any discrete point on the filament each second?

How far do the electrons travel within the tungsten filament per cycle? Assume the filament is perfectly uniform, that the heat in the filament is evenly distributed, and that the filament is 348mm in length with a diameter of 46µm.

Source: https://commons.wikimedia.org/wiki/File:Filament.jpg

Hint: What do electrons and rally cars have in common?

The challenge answer will be published in the next issue of *SHIFT LEFT*.



Resource Links

Keysight EDA Software

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Keysight SystemVue LinkedIn Group

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