PIC Studio

Integration with Foundry Ecosystem Accelerating End-to-End

Silicon Photonics Chip Development

https://www.latitudeds.com/

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LATITUDE DESIGN SYSTEMS

ENLIGHT TECHNOLOGY
恩萊特科技股份有限公司

01 Introduction

PIC Studio: A Unified Flow from Component, Circuit to System Design

Optoelectronic * Design Process

Optoelectronic System/Heterogeneous Integration/CPO
- Single-mode/multi-mode/DSP/BER/TDECQ, etc.

Circuit Design (Compound/Silicon Photonics)
- Layout
- Schematic
- Schematic Driven Layout (SDL)
- front-end/back-end simulation

Process/Component Design and Solver
- Process Simulation
- Active/passive component simulation
- PCell Design/Symbol Design/Model Creation

PIC Studio

System Level Simulation
pSim Plus
- Fiber optic simulation
- BER/DSP/TDECQ analysis
- System-level DSP for long-haul

Circuit Simulation
pSim
- PIC Circuit Simulator
- Multi-mode//Channel
- Frequency/Time Domain
- E/P Signal Processing & Tools
- Python3 & SPICE Integration

DRC
pVerify
- DRC/Boolean/density verification
- Custom & FAB rules
- PhotoCAD integration (chamfering/auto-repair)

Schematic
pLogic
- SDL/Circuit Simulation Entry
- Component Parameter Control
- Photonic Link Routing Control
- Metal Link
- Cross-probe
- Visible Routing Details
- E/P Integration Support

SDL
Advanced SDL
- Python Layout Scripts
- 3-in-1 GUI
- Front/Back-end Simulation Support

Windows Linux

Layout
PhotoCAD
- Python3 Environment
- Precise Complex Layout
- Auto-routing for waveguides
- Photonic Path Control
- E/P Integration
- Generic PDK Example

Solver
pMaxwell
- Interfaces: Ansys Lumerical, Comsol, Silvaco
- FDTD & RCWA Solvers

PIC Studio
- **pSim**
- **pSim Plus**
- **PhotoCAD**
- **Advanced SDL**
- **pLogic**
- **pMaxwell**
- **pVerify DRC**

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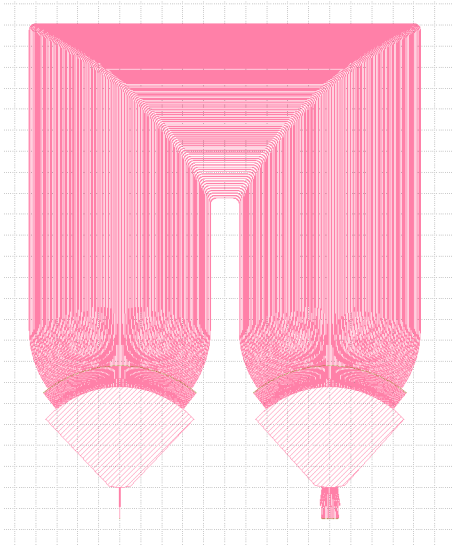
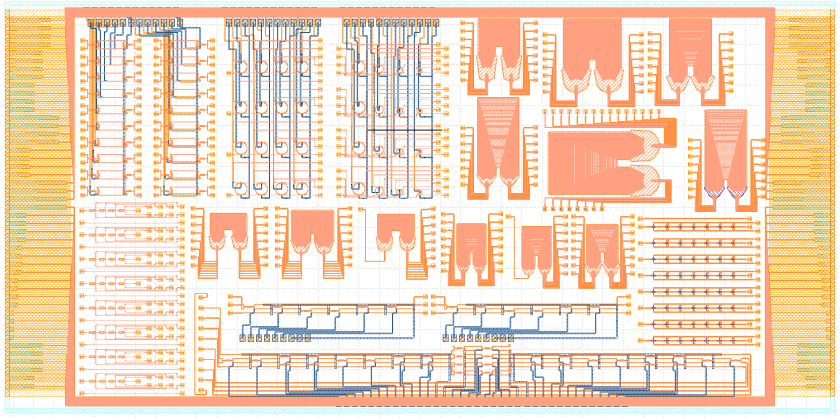
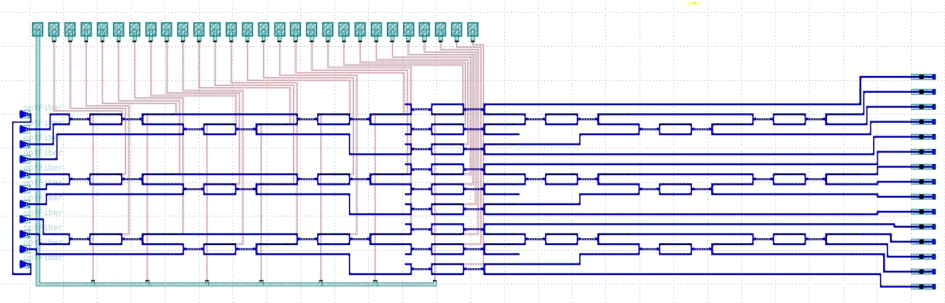
PhotoCAD – PIC Layout Design Automation



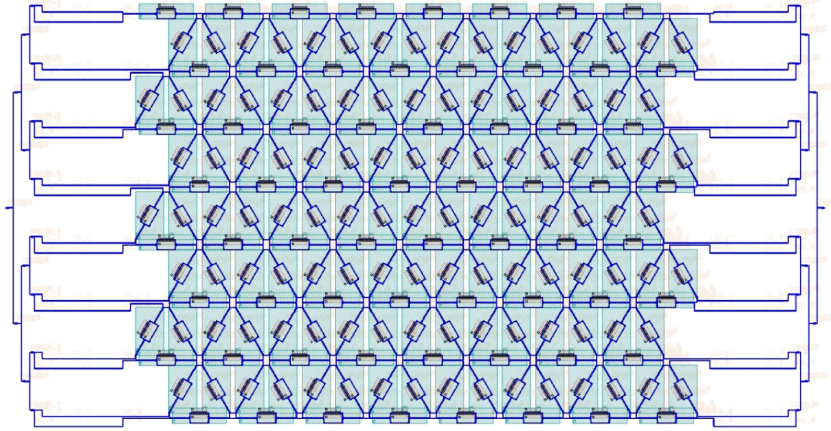
AWG (Arrayed Waveguide Grating)



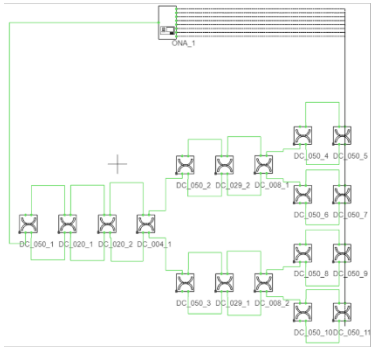
Foundry PDK



Optical Convolution Matrix Unit

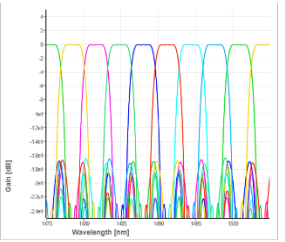


Programmable Photonics

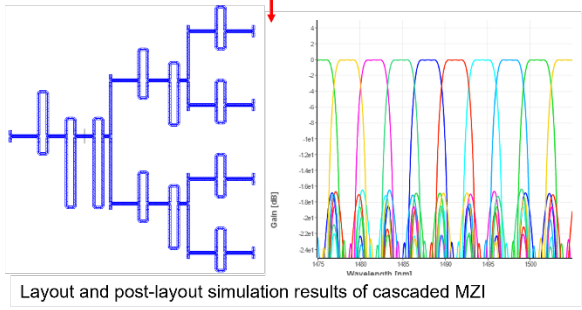


Cascaded MZI Schematic

After the schematic is completed, run a pre-layout simulation to check the performance



Pre-layout simulation results of cascaded MZI



Layout and post-layout simulation results of cascaded MZI

Pre-Layout and Post-Layout Photonic Circuit Simulation

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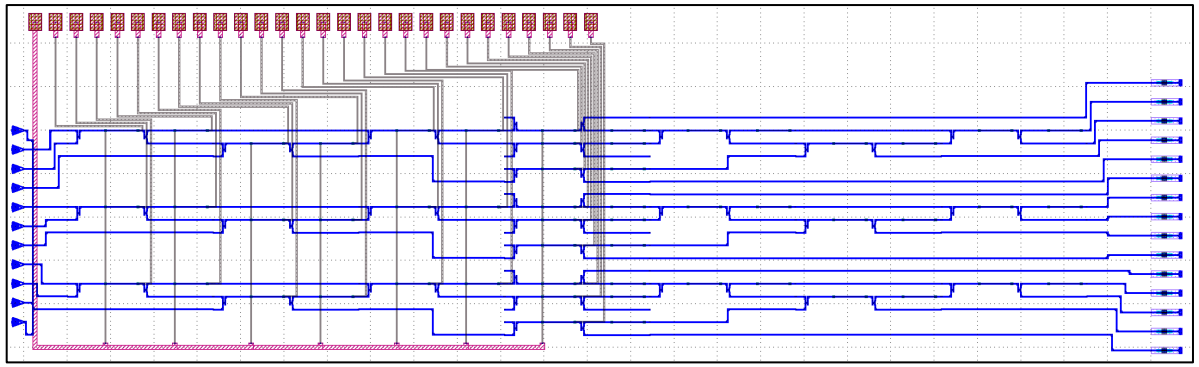
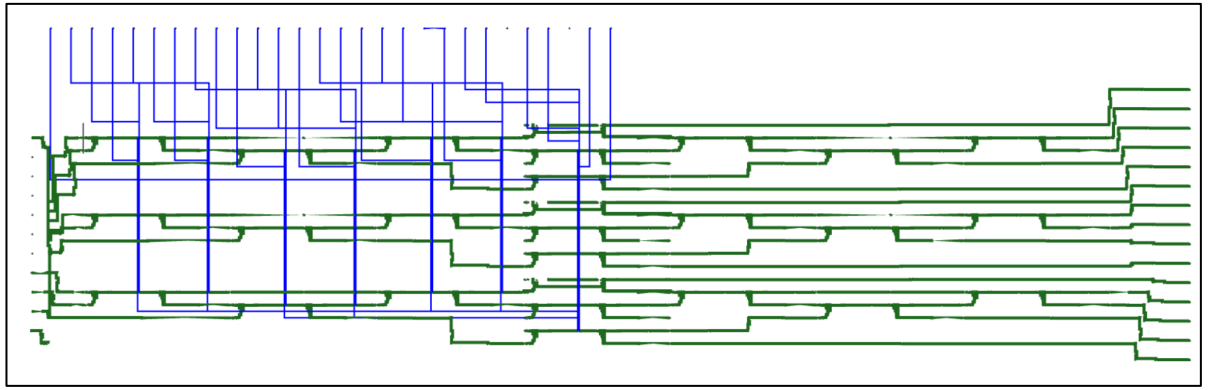
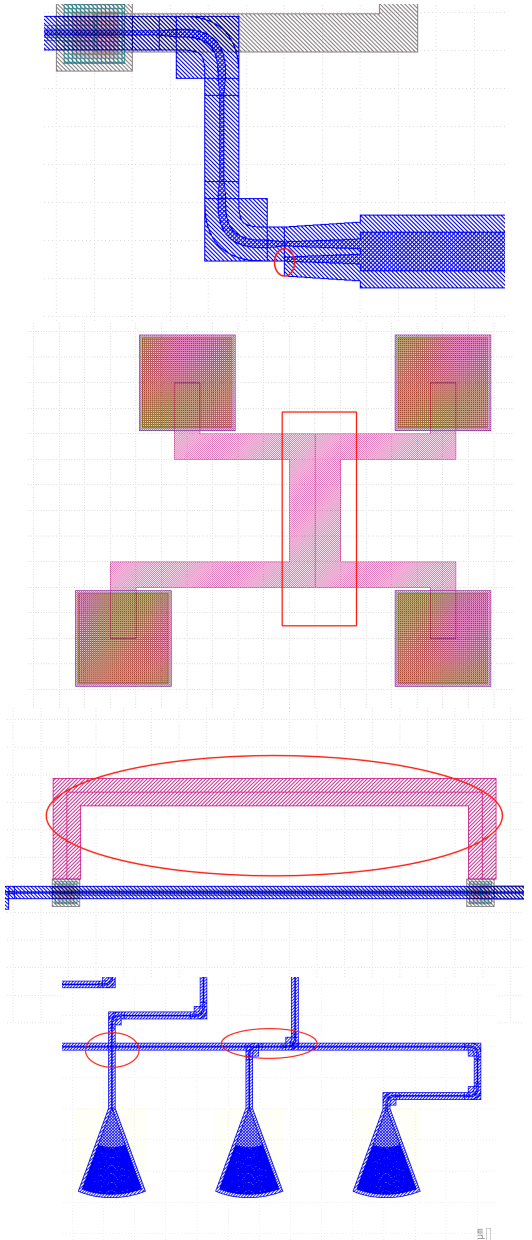
Advanced SDL – LVS Check



Netlist and Schematic Generation





LVS report highlighting abnormal connection

Floating Port

optical

Mmi_3: op_2

electrical

Phs_5: ep_0, ep_1

Multi-connection

MC1: pad_2:ep_1 | pad_3:ep_1 | phs:ep_1

MC2: ***:ep_1 | **:ep_1 | ***:ep_1

Short circuit

SC1: PHS_2:ep_1|ep_2

SC2: ***_3:ep_1|ep_2

Waveguide crossing

WC1: GC_1:op_0 | GC_2:op_0 | GC_3:op_0

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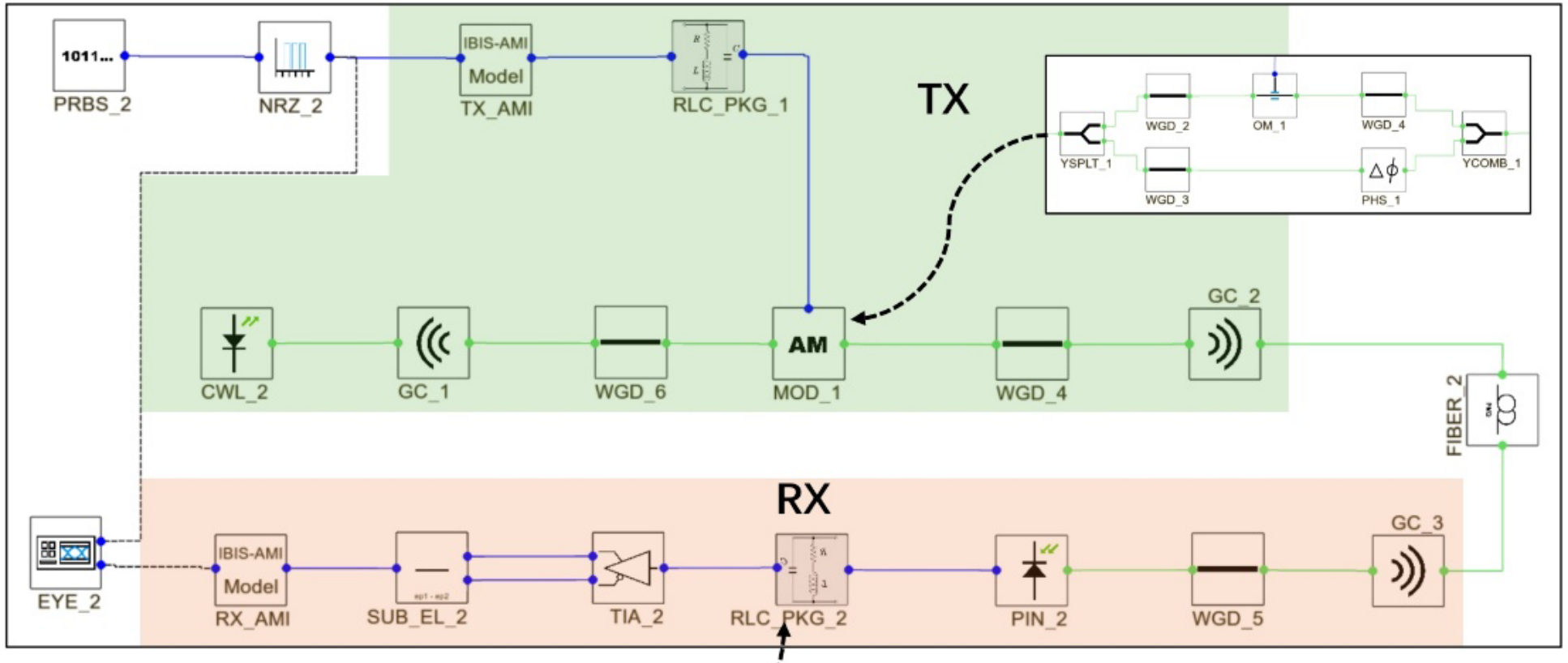
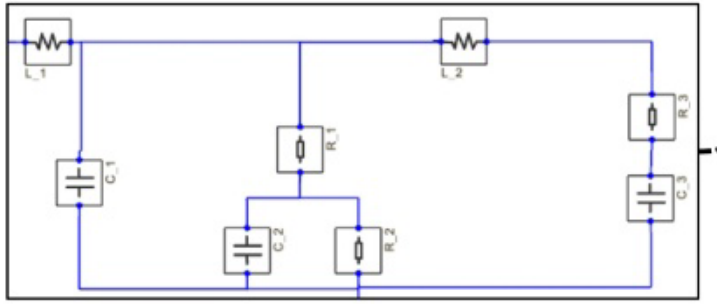
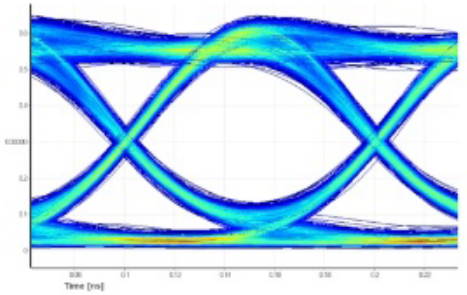
02

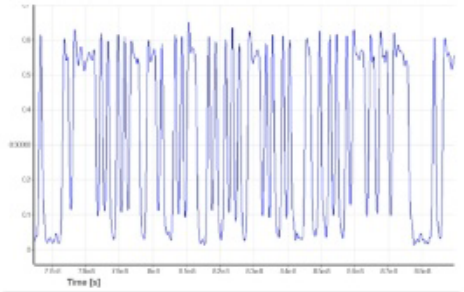
System Level Design

pSim Plus Electronic-Photonics End-to-End Simulation

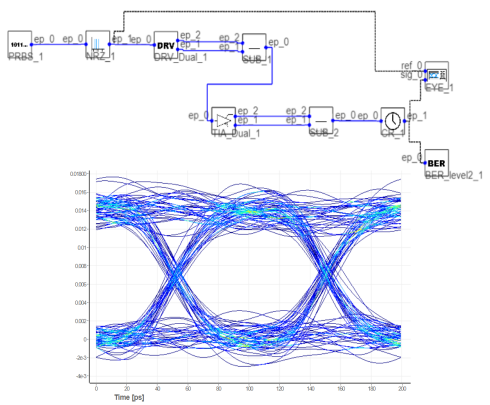




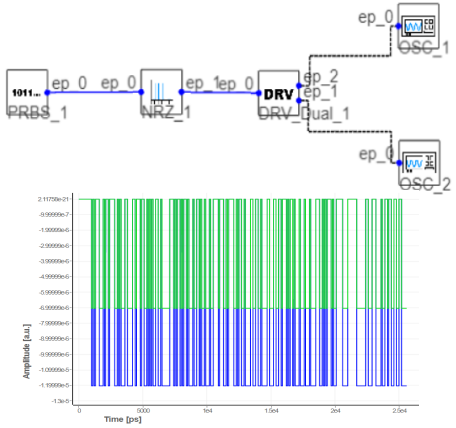




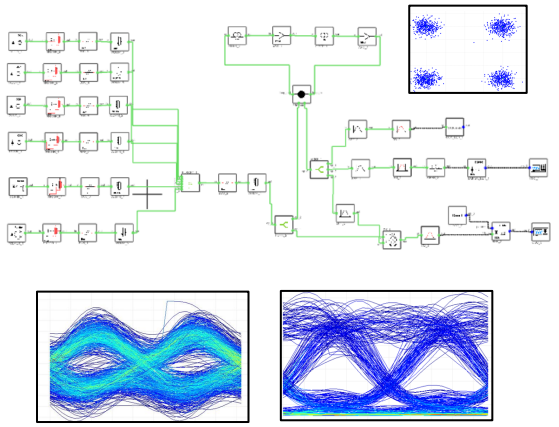
pSim Plus System-level Simulation (with DSP, Fiber, and Electronics)



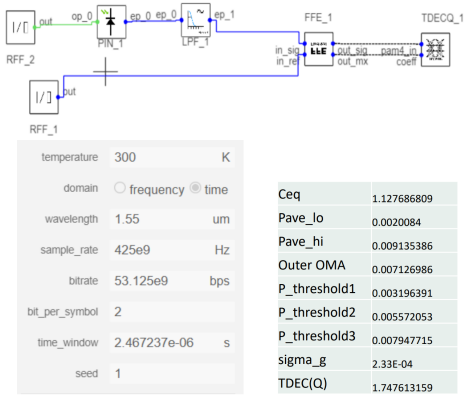
TIA Circuit Simulation



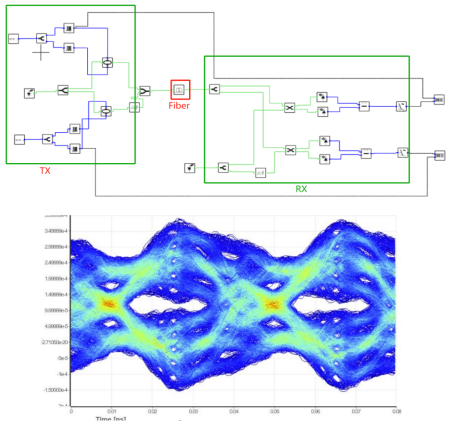
Driver Circuit Simulation



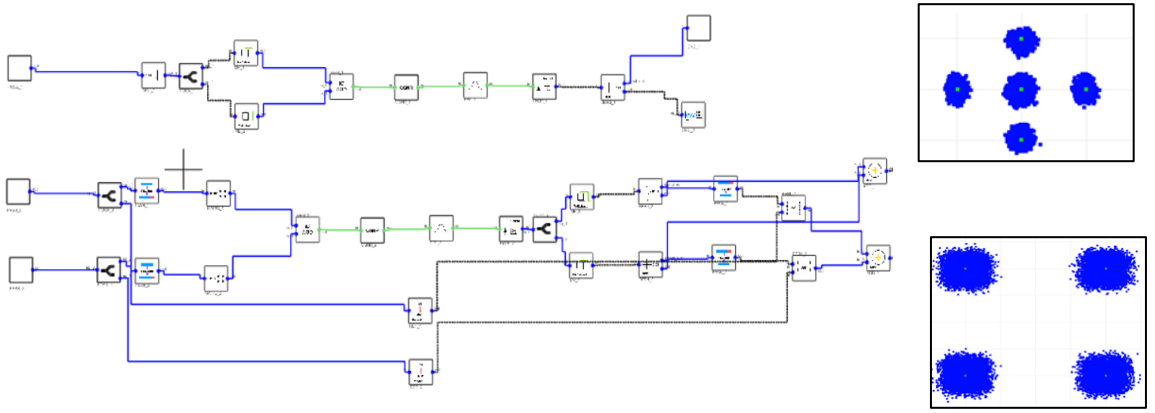
Multi-Channel WDM Long-Haul Fiber Simulation



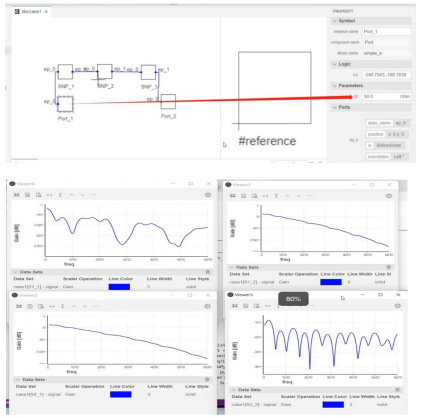
FFE Signal Equalization + TDECQ Signal Quality Evaluation



NLS+PMD Simulation for Fiber Optics



PS-QPSK + FEC Coherent Transmission Links



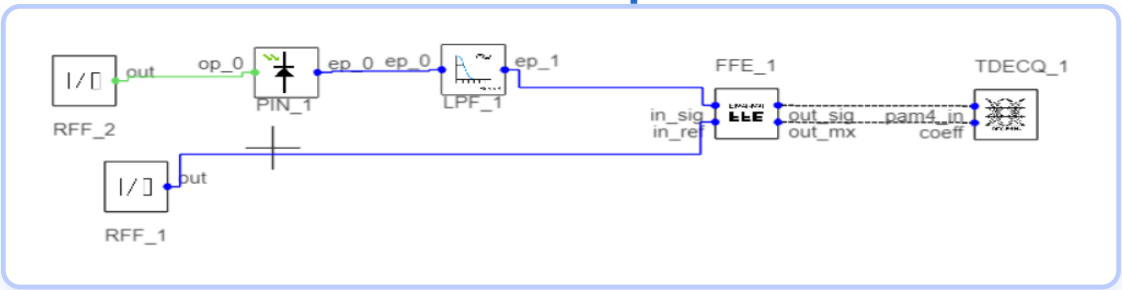
RLCG Support for Circuit Simulation and SNP files.

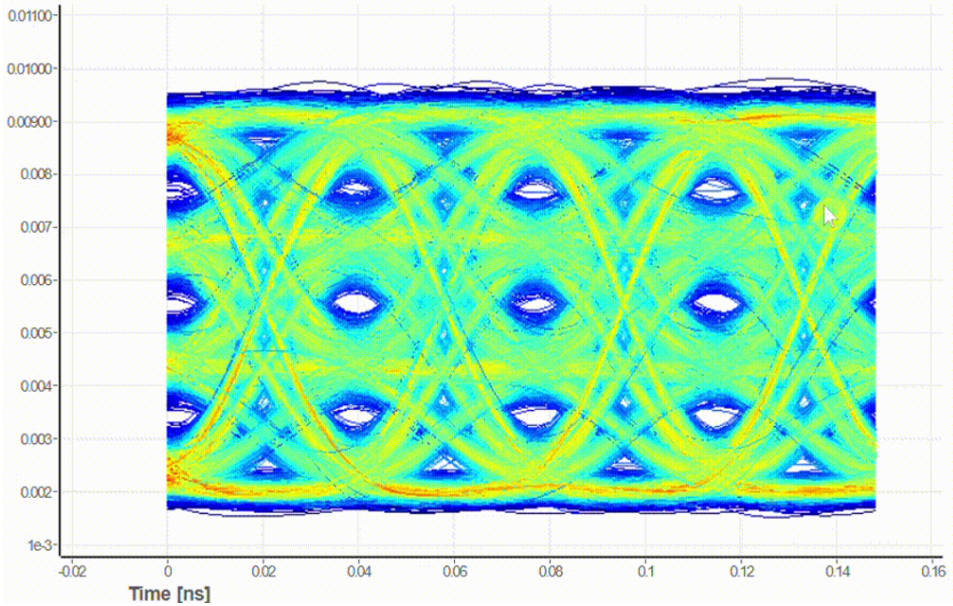
pSim Plus TDECQ Example

- Optical and reference sources are loaded and converted to electrical signals by PD, then equalized by an electrical equalizer, and finally analyzed by TDECQ.

temperature	300	K
domain	○ frequency ◉ time	
wavelength	1.55	um
sample_rate	425e9	Hz
bitrate	53.125e9	bps
bit_per_symbol	2	
time_window	2.467237e-06	s
seed	1	

TDECQ example





Ceq	1.127686809
Pave_lo	0.0020084
Pave_hi	0.009135386
Outer OMA	0.007126986
P_threshold1	0.003196391
P_threshold2	0.005572053
P_threshold3	0.007947715
sigma_g	2.33E-04
TDEC(Q)	1.747613159

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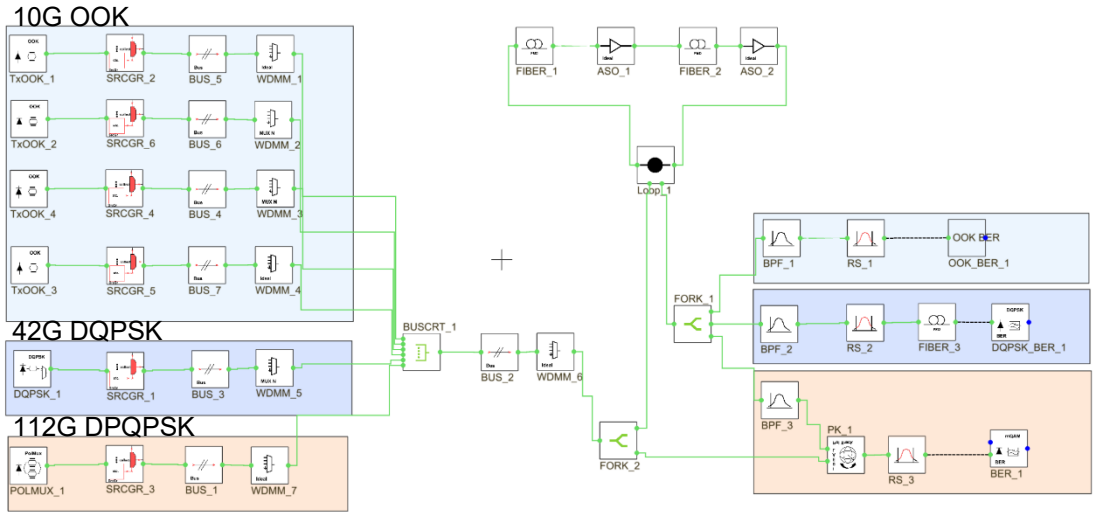
pSim Plus System-Level Design Scenarios

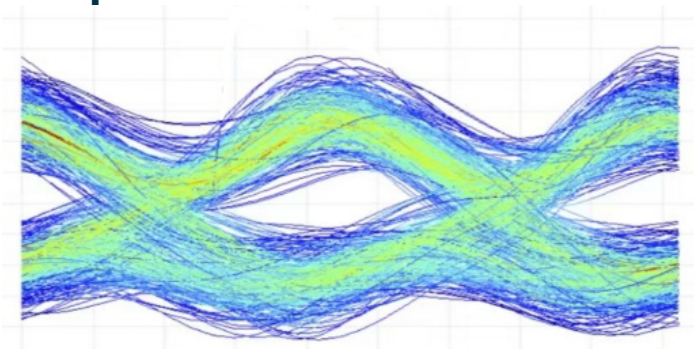
CWDM Single-Mode Long-Haul System

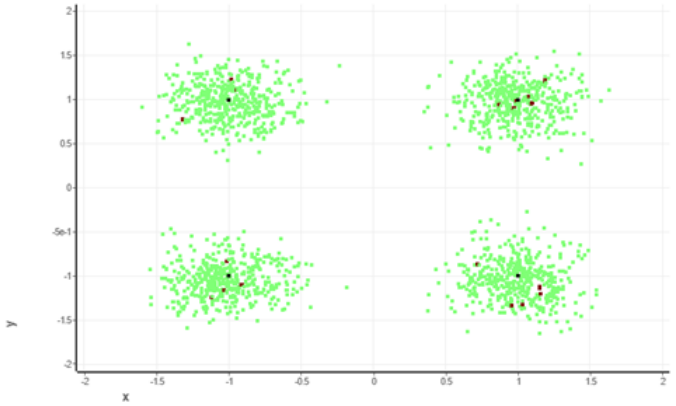


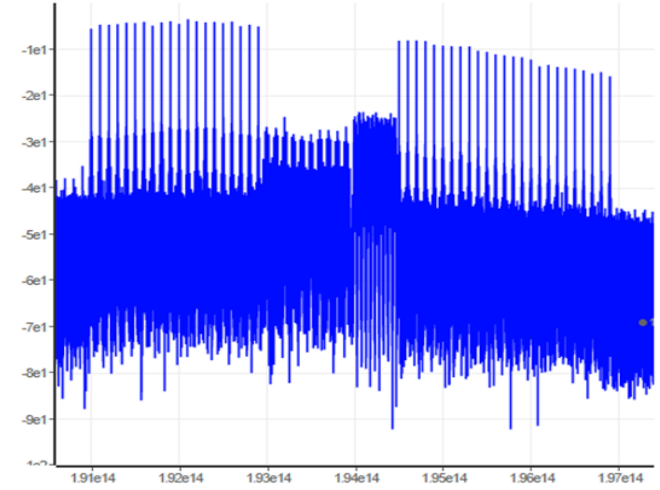
Simulation Description: CWDM single-mode long-haul system using OOK, QPSK, and DP-QPSK over 191–197 THz (6 THz bandwidth), transmitted **915 km** with **20 amplifier spans**.

Simulation Config: Optical noise from lasers and amplifiers is modeled over a **10 THz bandwidth** with ASE added, to assess impact vs. an ideal noiseless system.

pSim Plus Simulation







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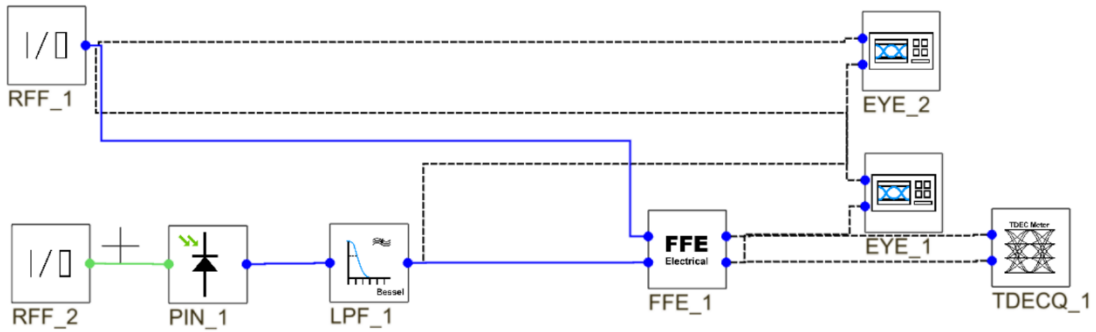
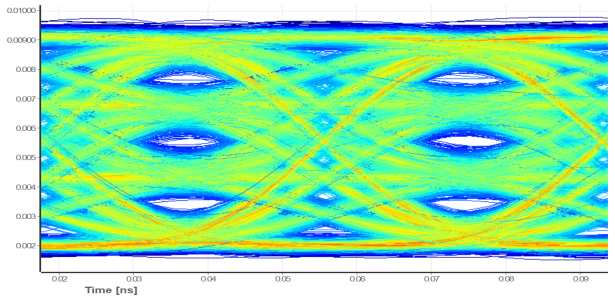
pSim Plus System-Level Design Scenarios

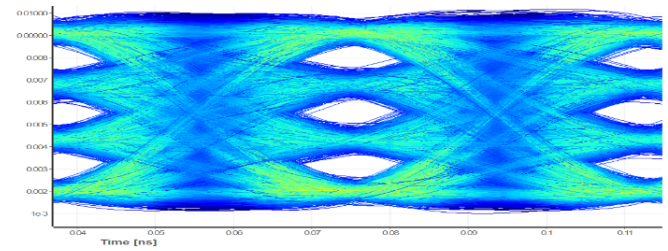
FFE Equalization and TDECQ Analysis

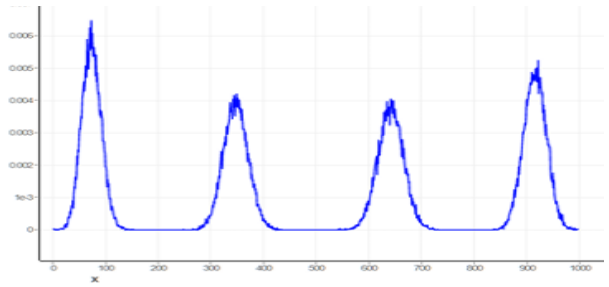


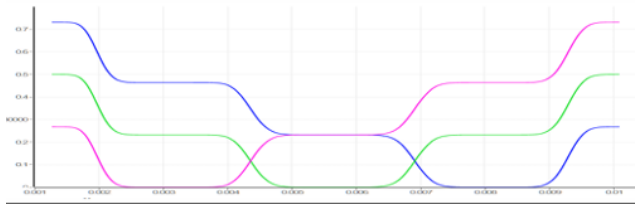
	VPI				pSim+	
Ceq	1.131854853	40s	*百分比+/-10%	≤5*ref	1.127069993	-0.004245397
Pave_lo	0.002007575		*百分比+/-5%	≤5*ref	0.0020084	0.000410655
Pave_hi	0.009137723		*百分比+/-5%	≤5*ref	0.009135386	-0.000255885
Outer OMA	0.007130148		*百分比+/-5%	≤5*ref	0.007126986	-0.000443717
P_threshold1	0.003167229		*百分比+/-5%	≤5*ref	0.007947715	0.60149191
P_threshold2	0.005572148		*百分比+/-5%	≤5*ref	0.005572053	-1.70557E-05
P_threshold3	0.007977568		*百分比+/-5%	≤5*ref	0.003196391	-1.495805011
sigma_g	0.000233584		*百分比+/-5%	≤5*ref	0.000232902	-0.002925525
TDEC(Q)	1.732323646		±0.05	≤5*ref	1.74317363	0.00622427

pSim Plus Simulation









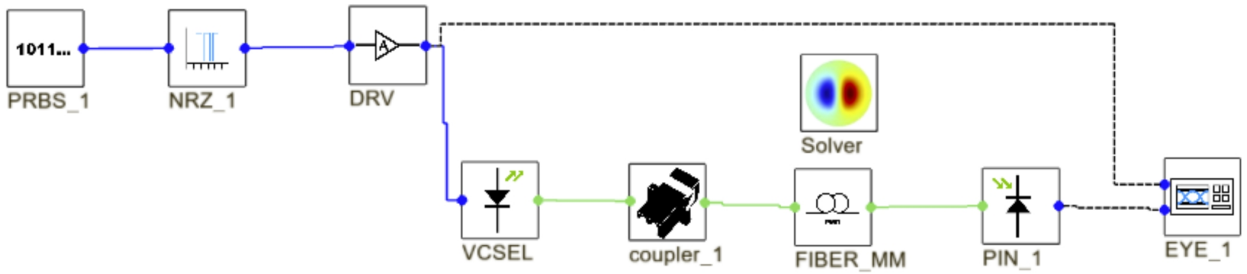
Simulation Description:
The circuit demonstrates loading **external data** as both optical and electrical signal sources. At the receiver, **FFE equalization** is applied, followed by **TDECQ analysis for a four-level signal**.

LATITUDE DESIGN SYSTEMS

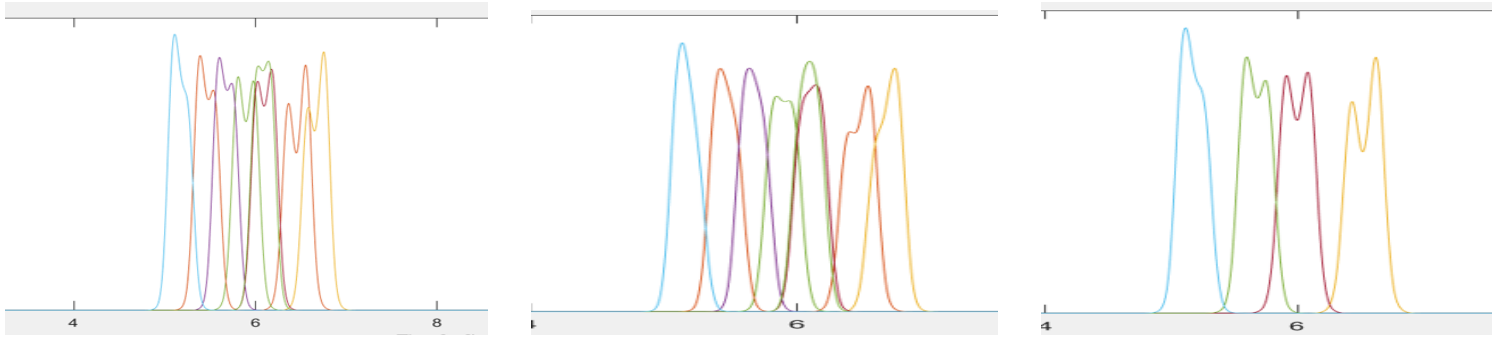
pSim Plus System-Level Design Scenarios

Multimode Fiber Short-Distance Application

Simulation Description: Multimode fiber model with configurable index profile, mode count, PMD, coupling, and nonlinearity.
Pulse distortion analyzed under various settings, with results **matching VPI**.



pSim Plus Simulation



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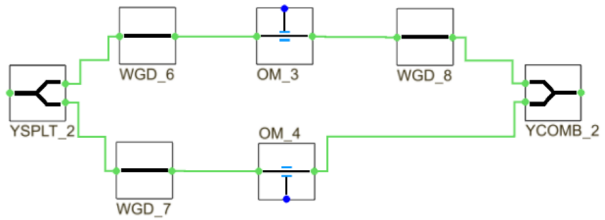
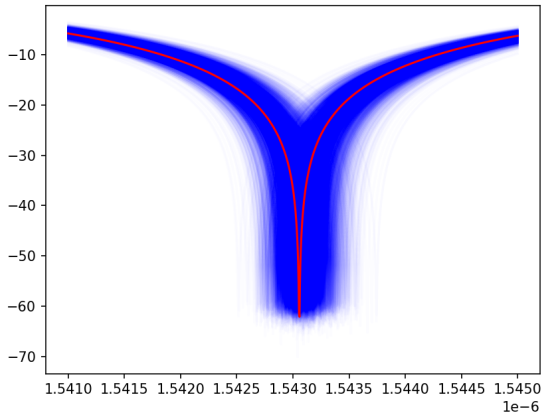
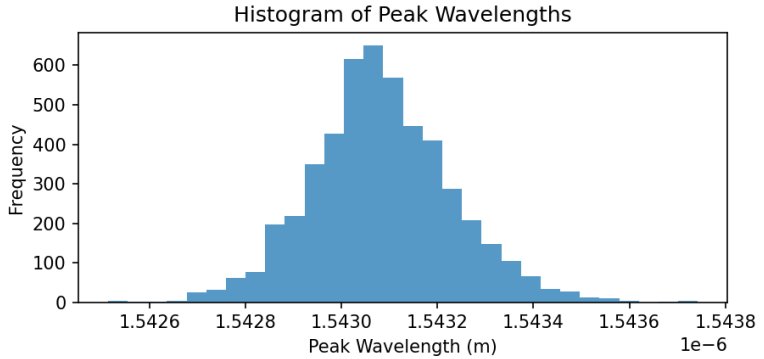
pSim Plus Monte-Carlo Simulation to Estimate Process Variation

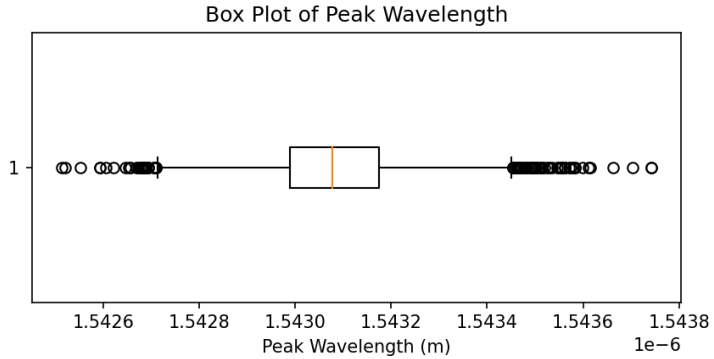


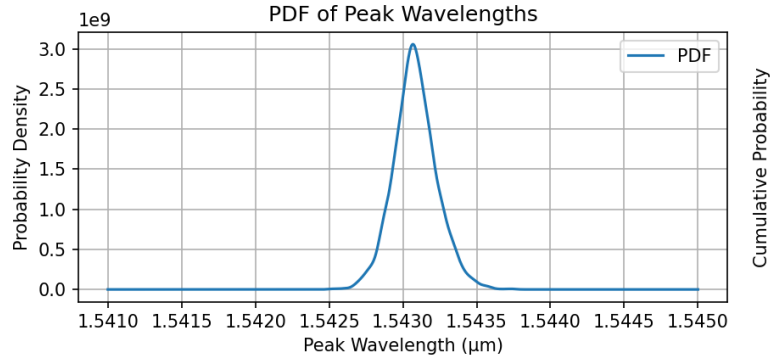


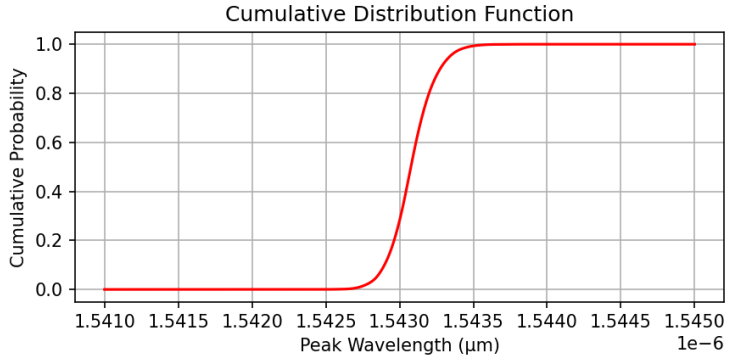
Statistical upper/lower arms' refractive indices →
Statistical waveguide loss →

```
for _ in range(iterations):
    neff_upper = 2.435 + abs(np.random.normal( loc: 0,  scale: 0.0001))
    neff_lower = 2.422 + abs(np.random.normal( loc: 0,  scale: 0.0001))
    loss = 200 + np.random.normal( loc: 100,  scale: 50)
```









The GUI script runs Monte Carlo simulations, then analyzes the results to generate the statistical charts shown on the right, revealing how device performance variations affect overall system performance.

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03

pVerify DRC

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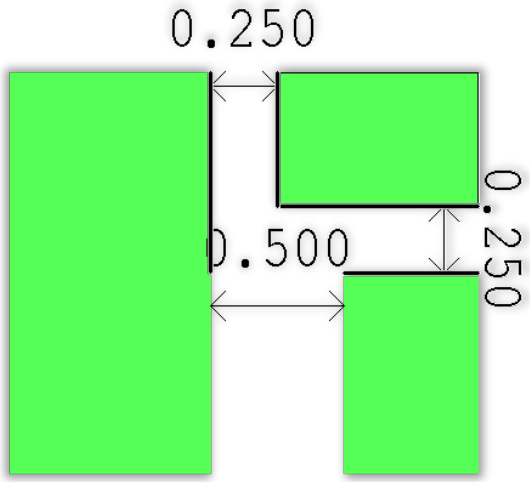
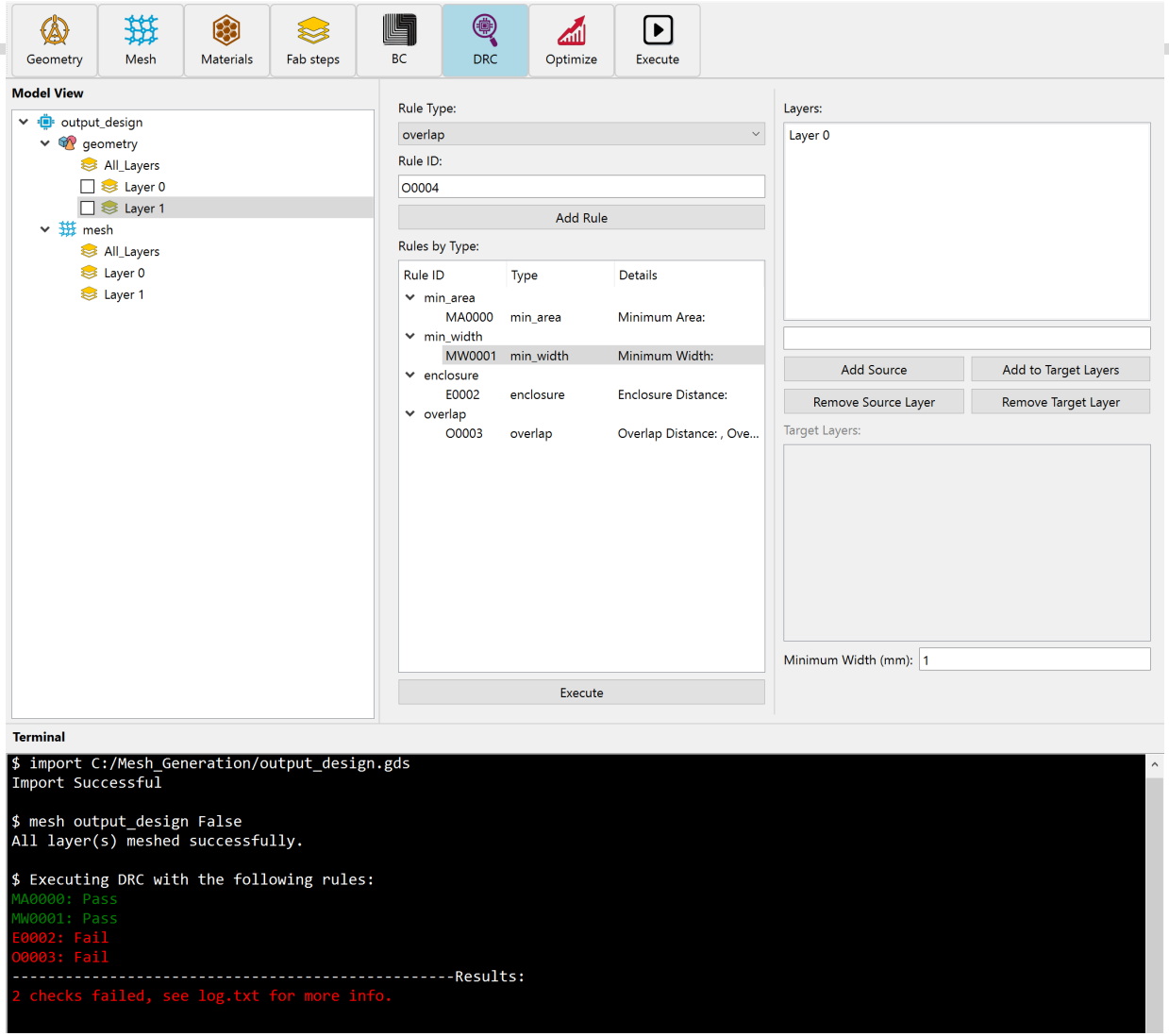
pVerify: Integrated Design Rule Check for PIC

- The fully customized design rules include rule types, target layers, and rule data
- Rule Types: Exact Width, Minimum Width, Spacing, Enclosure, Overlap, Extension, Existence, and Density
- Using derived layers, auxiliary graphics can be implicitly generated to perform more complex design rule checks



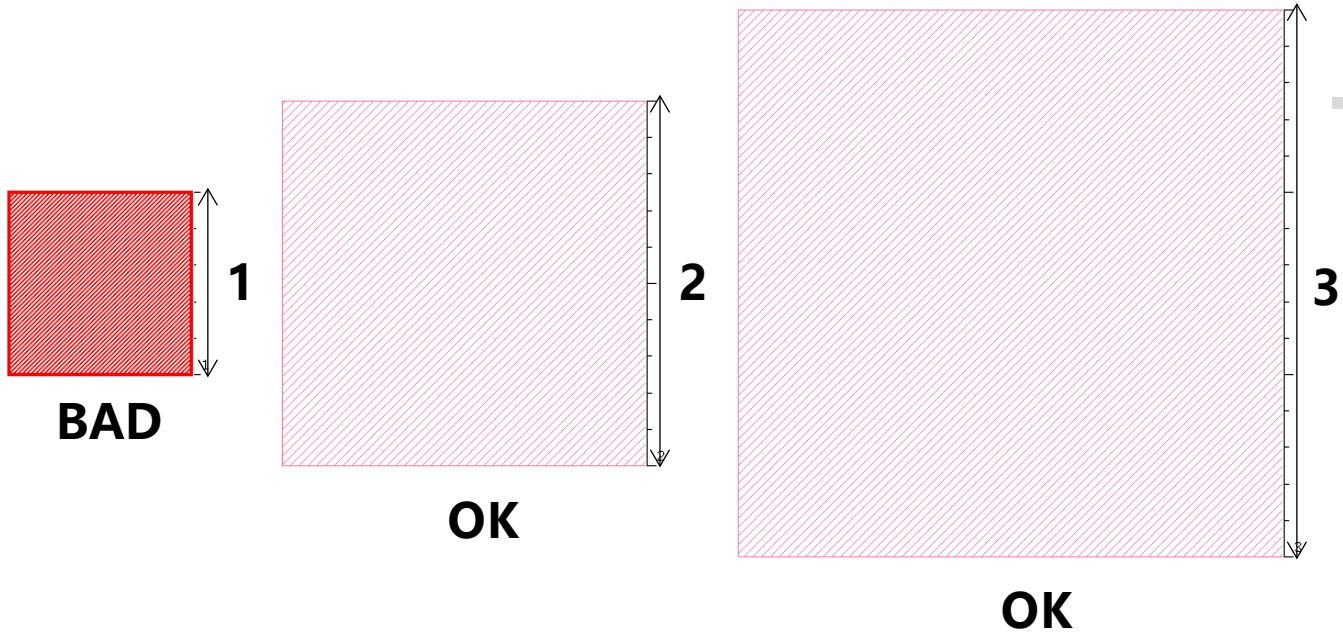


pVerify — A Powerful Yet Easy-to-Use DRC Tool

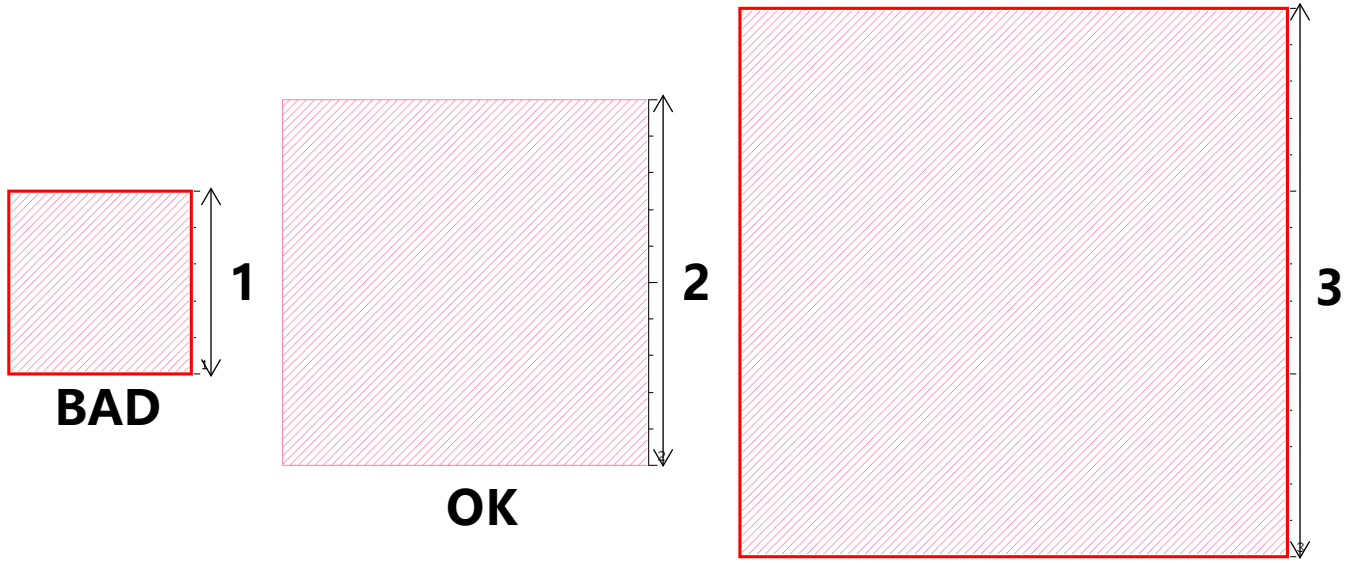
- Basic DRC Checks
  - Min. Width
  - Exact Width
  - Spacing
  - Area
- Layer Generation Methods
  - Boolean Operations
  - Sizing
- Acute Angle
  - Acute Angle
  - Acute Angle Patch
- Extended Geometrical Checks
  - Enclosure
  - Separation
  - Inside
  - Outside
  - Not Interacting
  - Overlap
- Density
  - Local
  - Global

Basic DRC Checks

- Min. width:
  - Checks the minimum width of all specified objects. Any objects with widths smaller than the specified valu will be flagged.
  - example: Min. width = 2 µm

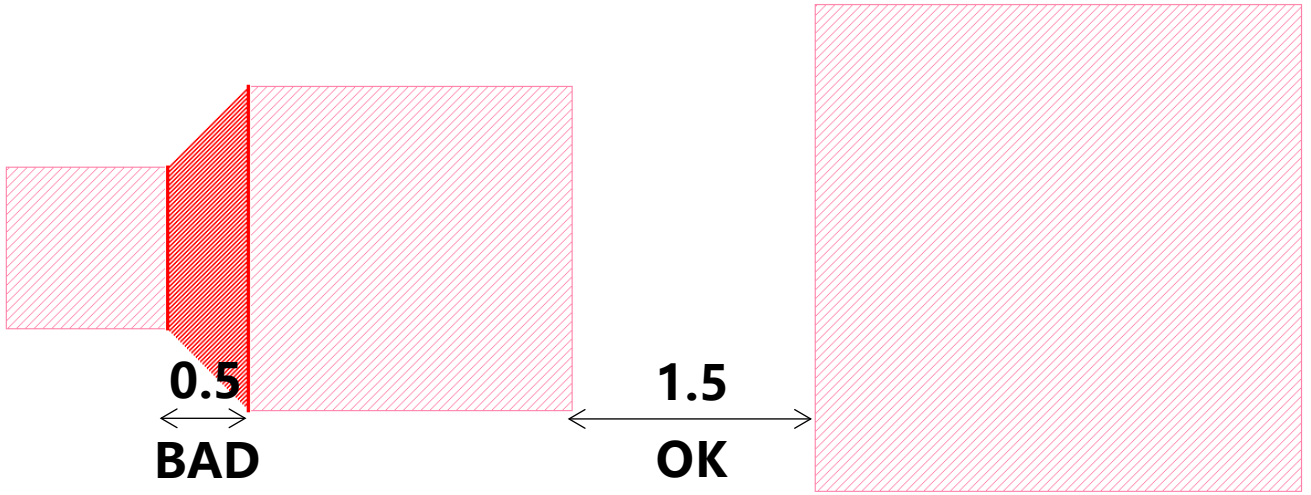


- Exact width:
  - Checks the width of all specified objec Any objects that do not match this exa width will be flagged.
  - example: Exact width = 2 µm

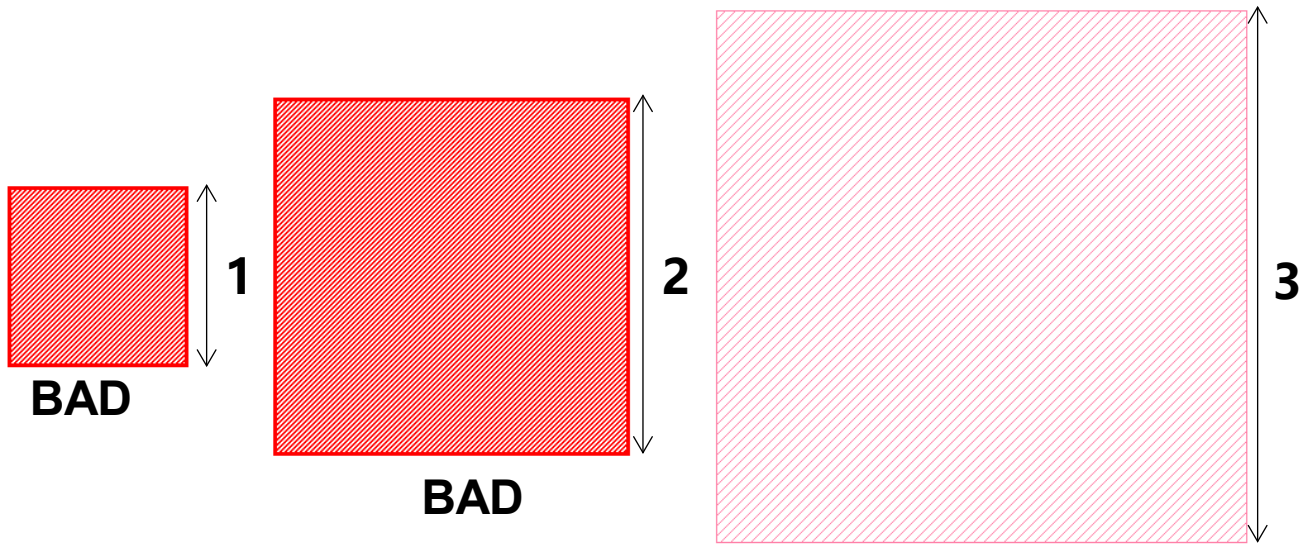


Basic DRC Checks

- Spacing:
  - Checks the minimum spacing between objects on the same layer. Any spaces smaller than this value will be flagged.
  - example: Min. spacing = 1 µm

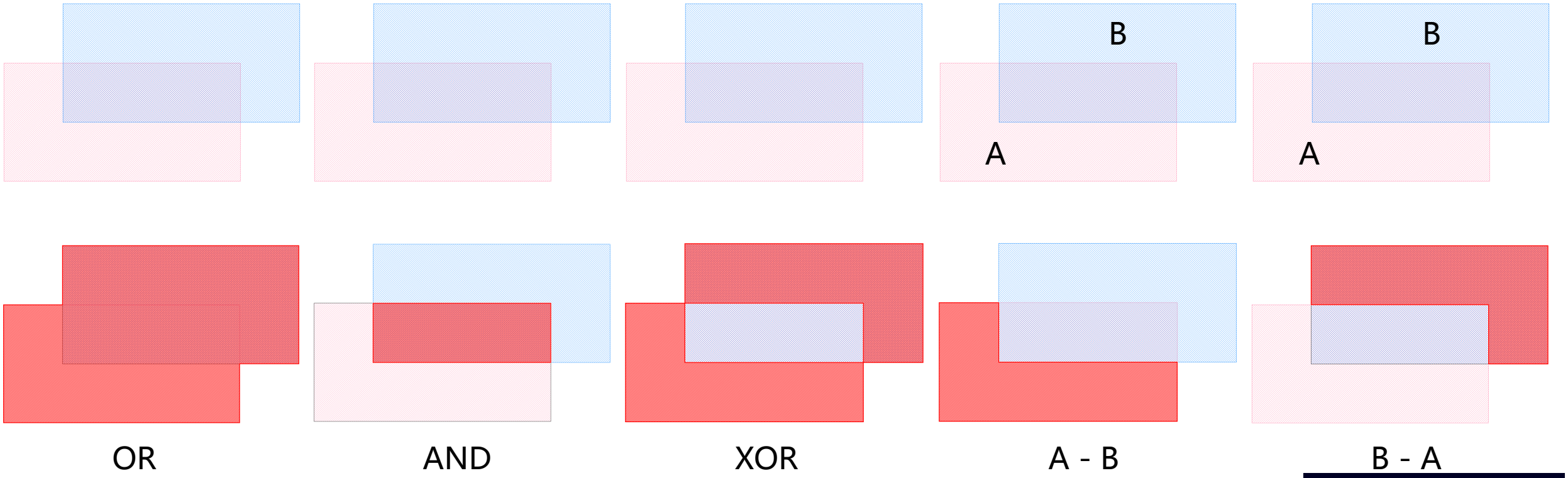


- Area:
  - Checks the minimum area of polygons. Any polygons with areas smaller than this value will be flagged.
  - example: Min. area = 5 µm^2



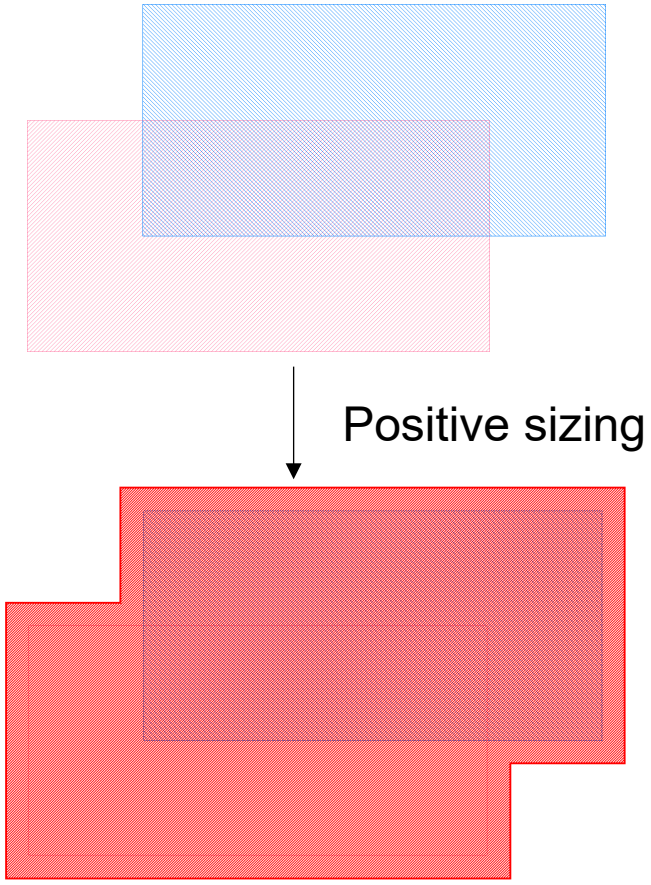
Layer Generation Methods

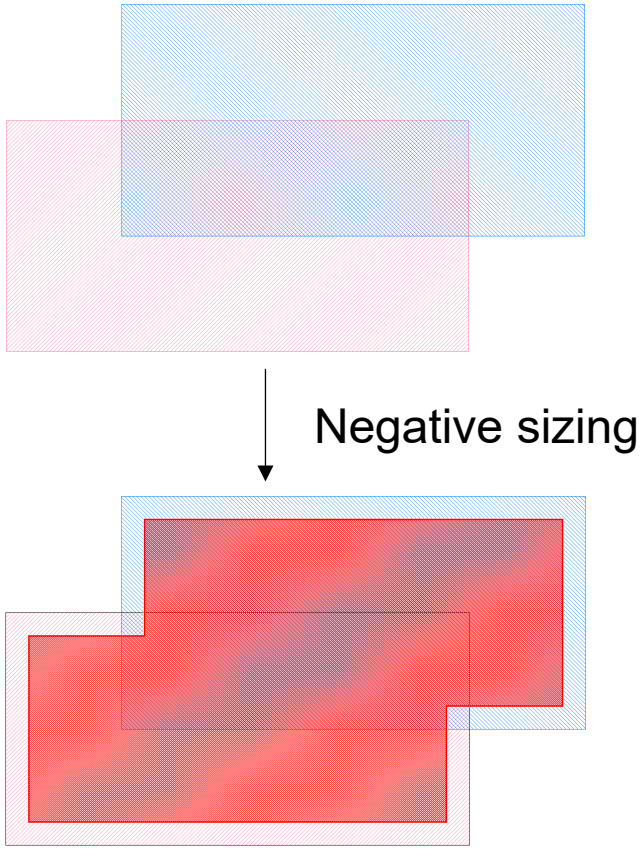
- Boolean Operations:
  - Perform Boolean operations between layers
    example: Layer A & Layer B, Layer A - Layer B, etc.



Layer Generation Methods

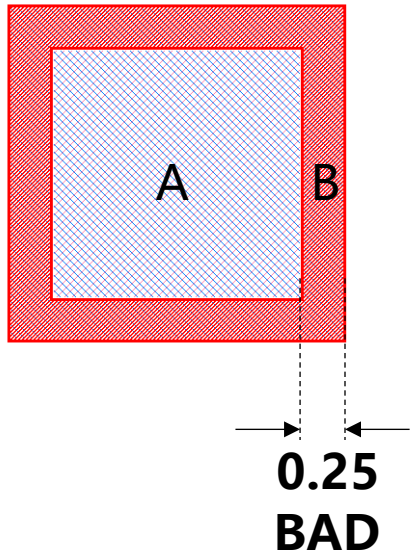
- Sizing:
  - Scale (enlarge or shrink) polygons

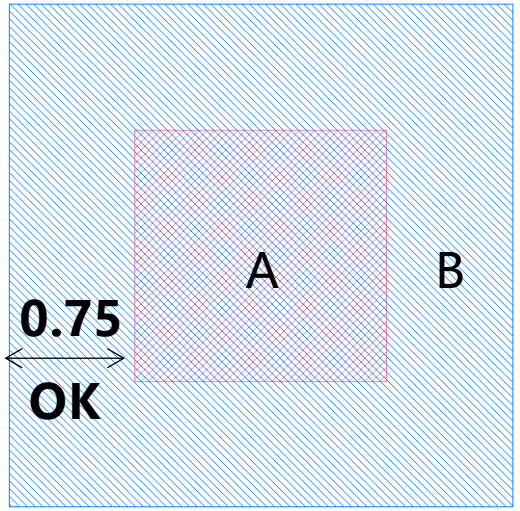




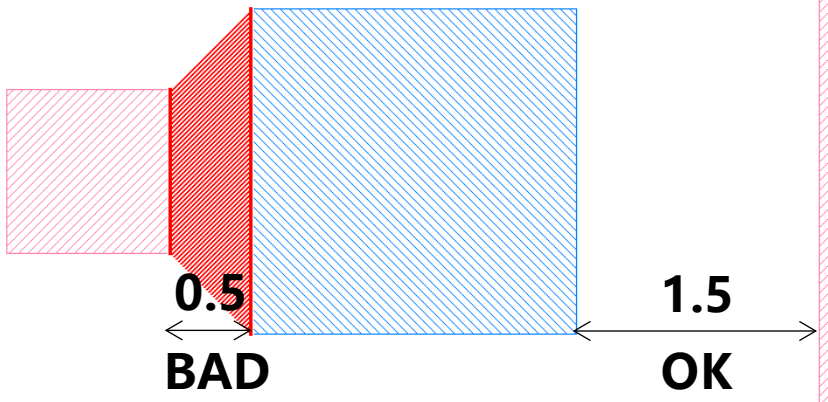
Extended Geometrical Checks

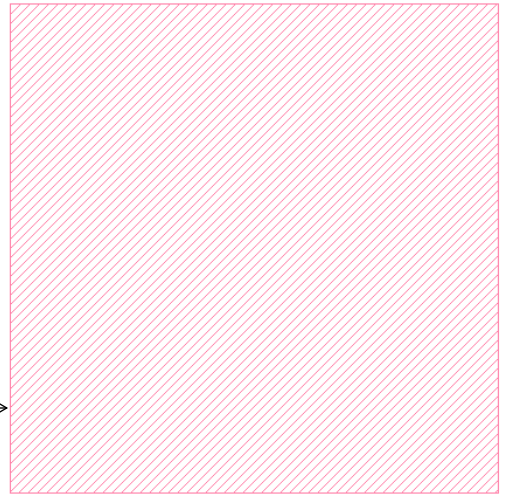
- Enclosure:
  - Check if a layer is surrounded by other layers, with a surrounding distance not less than a given value, and mark it if the distance is less than that value
  - example: Layer A Min. enclosure by Layer B = 0.5 μm
    (Layer A: red, Layer B: blue)





- Separation:
  - Check the minimum spacing between different layers, and mark areas where spacing is less than the specified value
  - example: Min. separation = 1 μm

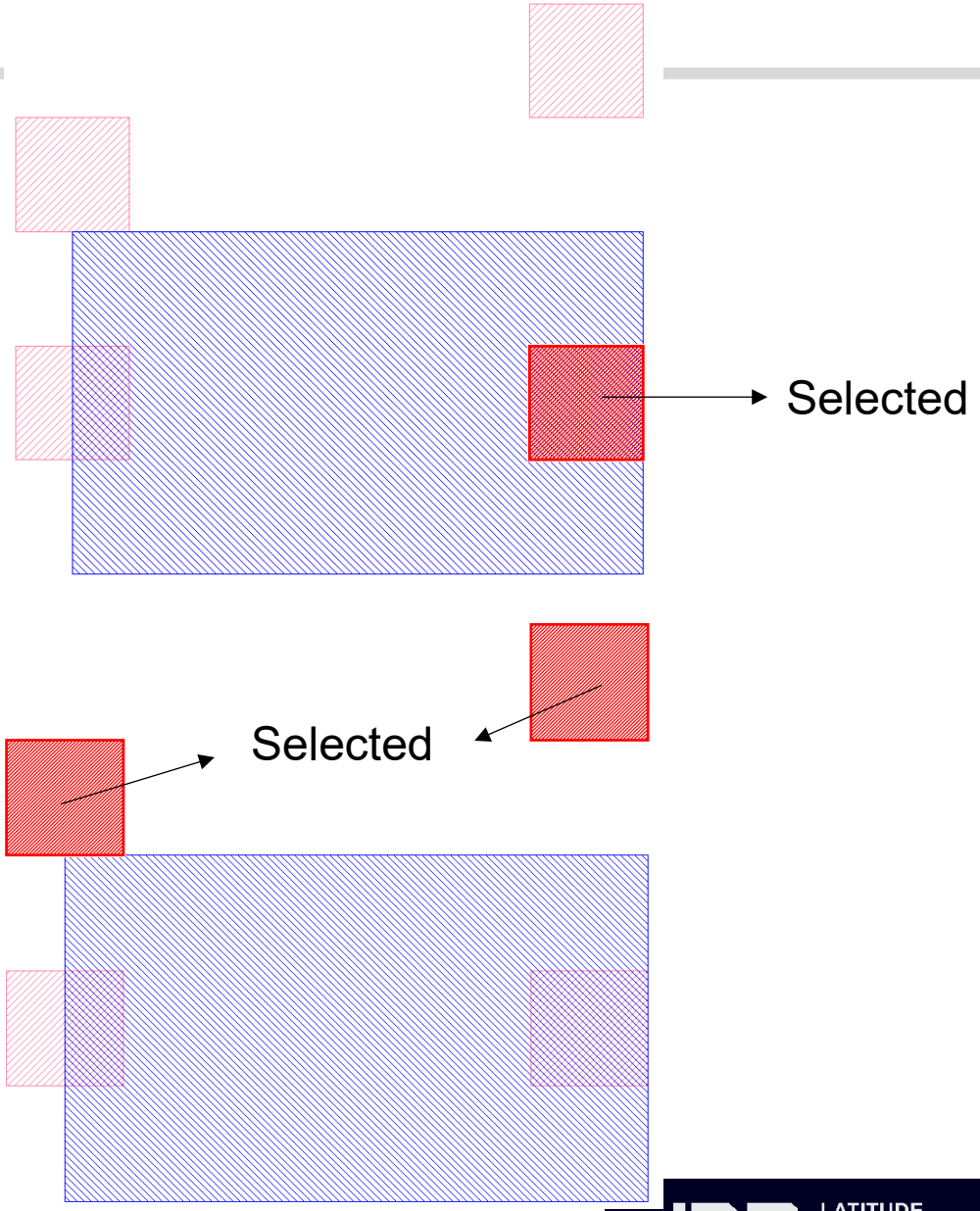




Extended Geometrical Checks

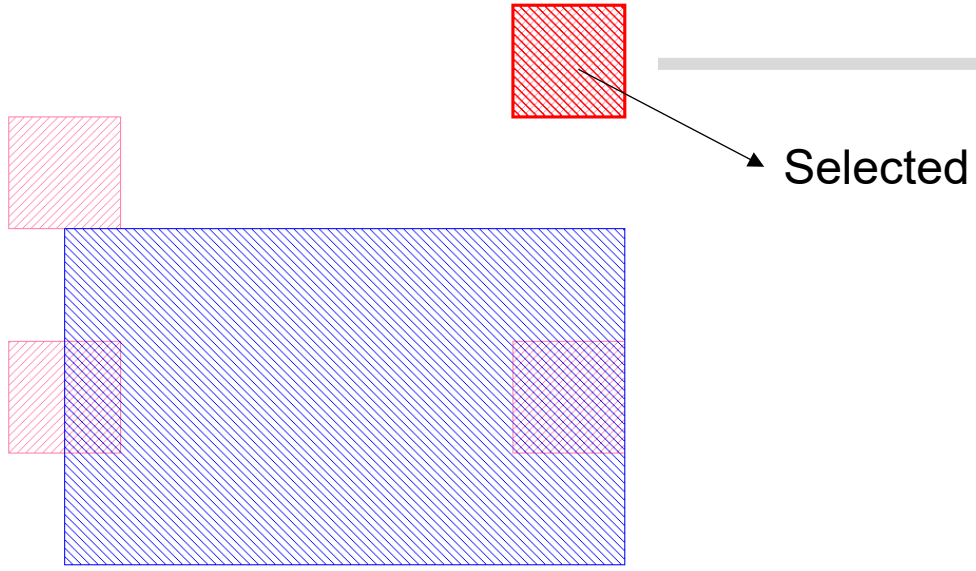
- Inside:
  - Select all polygons that are completely contained within polygons of another layer
  - example: Layer A inside Layer B
    (Layer A: red, Layer B: blue)

- Outside:
  - Select all polygons that lie completely outside of polygons on another layer
  - example: Layer A outside Layer B
    (Layer A: red, Layer B: blue)

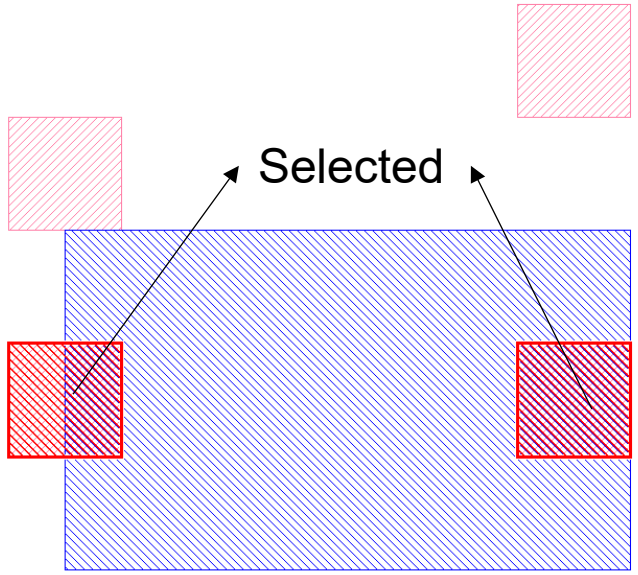


Extended Geometrical Checks

- Not interacting:
  - Select all polygons that have no contact or overlap with polygons on another layer
  - example: Layer A not interacting with Layer B
    (Layer A: red, Layer B: blue)



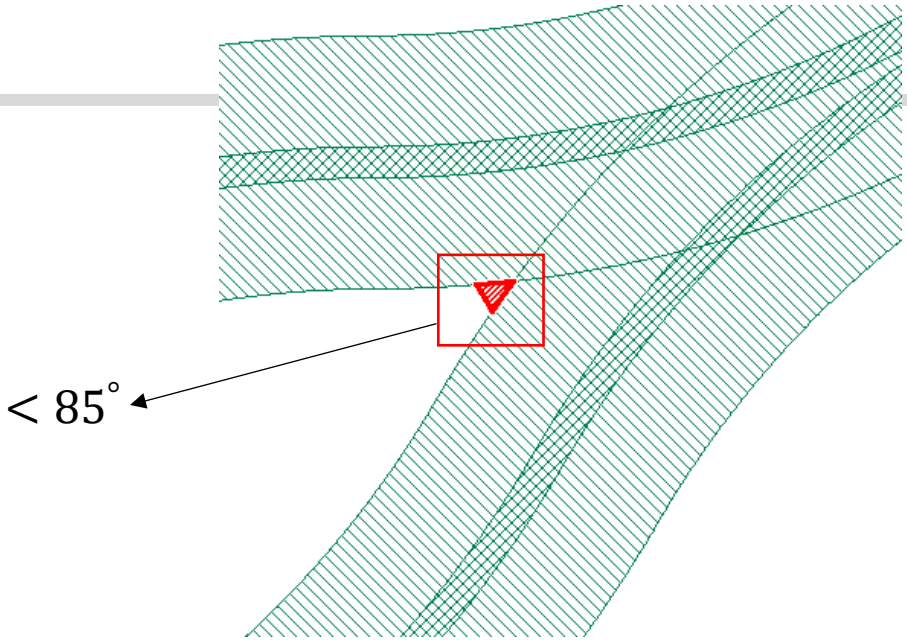
- Overlap:
  - Select all polygons that overlap with polygons on another layer
  - example: Layer A overlap with Layer B
    (Layer A: red, Layer B: blue)



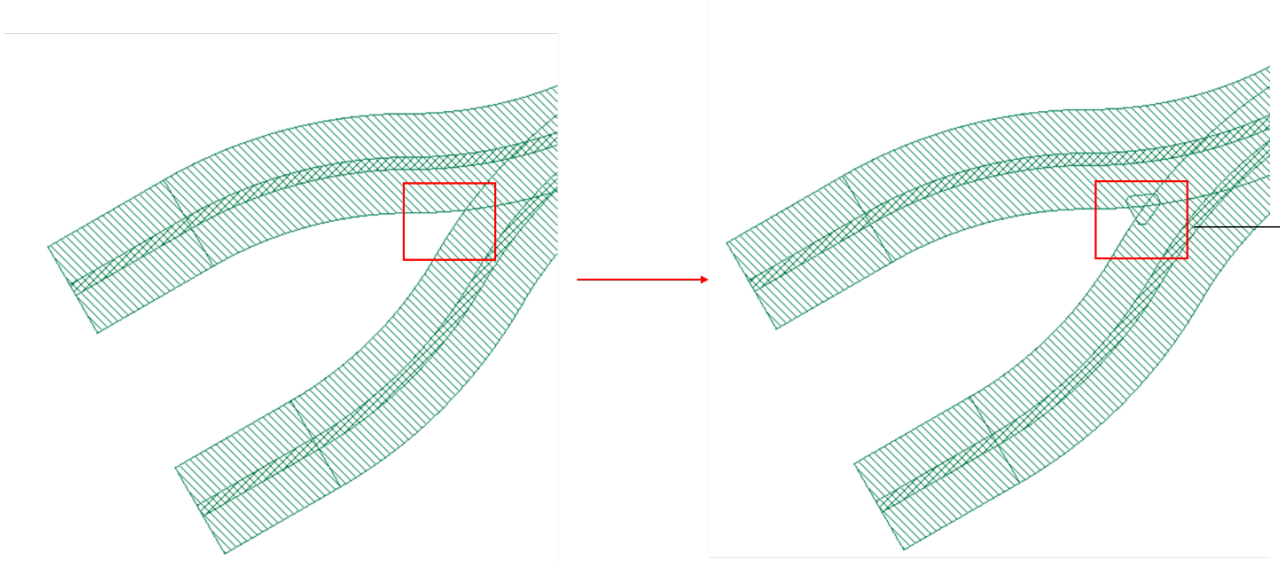
Acute Angle – Check and Repair

- Acute Angle:
  - Find acute angle regions on the layout where the angle is less than the input angle

example: Angle < 85 degrees is not allowed



- Acute Angle Patch:
  - Place a patch in the acute angle region to fix/repair the acute angle



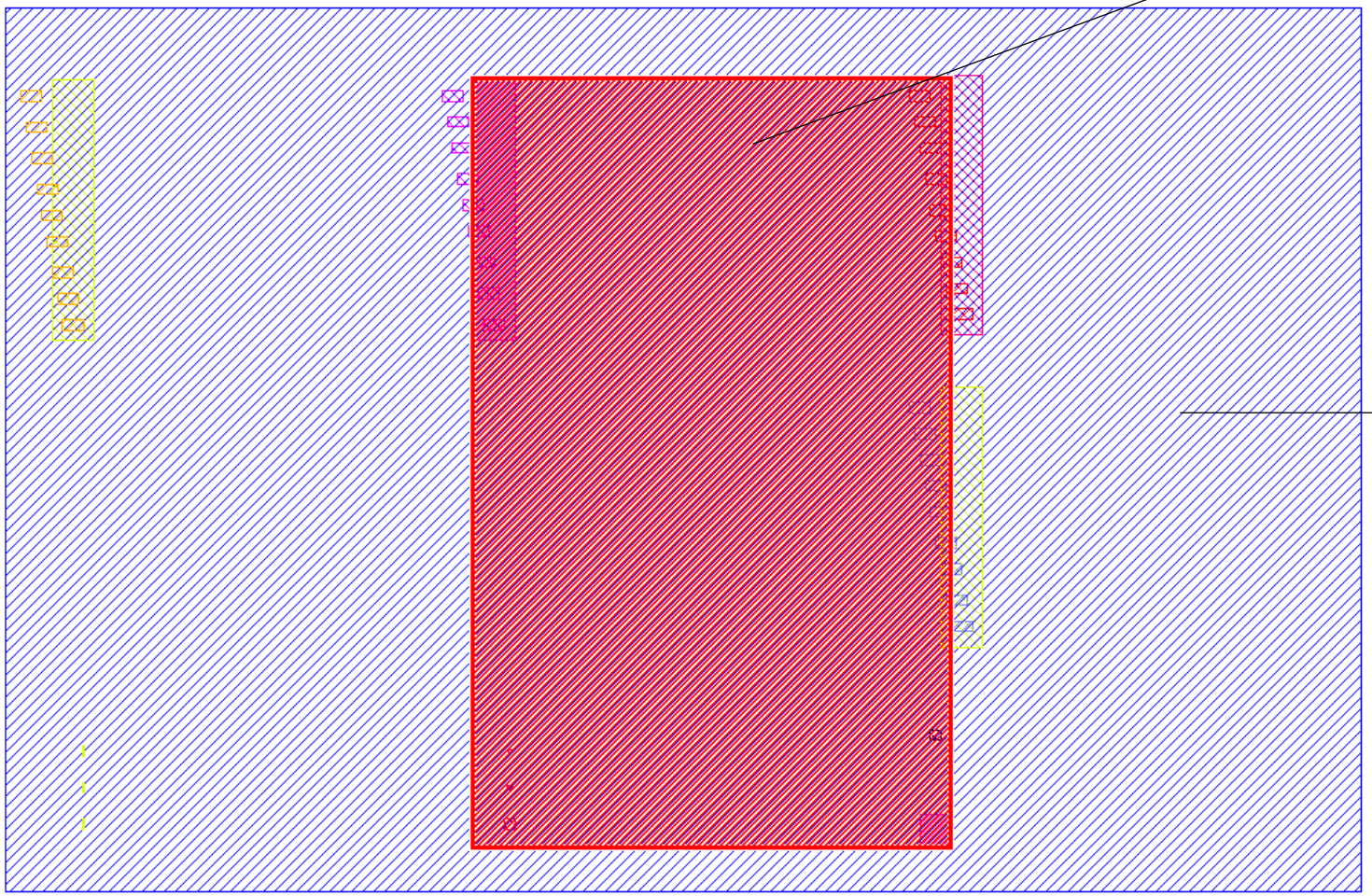
Patch sharp angles by adding patches of the same layer in the sharp angle region

Density Check

- Return regions where the density falls within a specified range
- example: 80 % ≥ Local density ≥ 20%

Local density > 80% or Local density < 20%

BAD



80 % ≥ Local density ≥ 20%

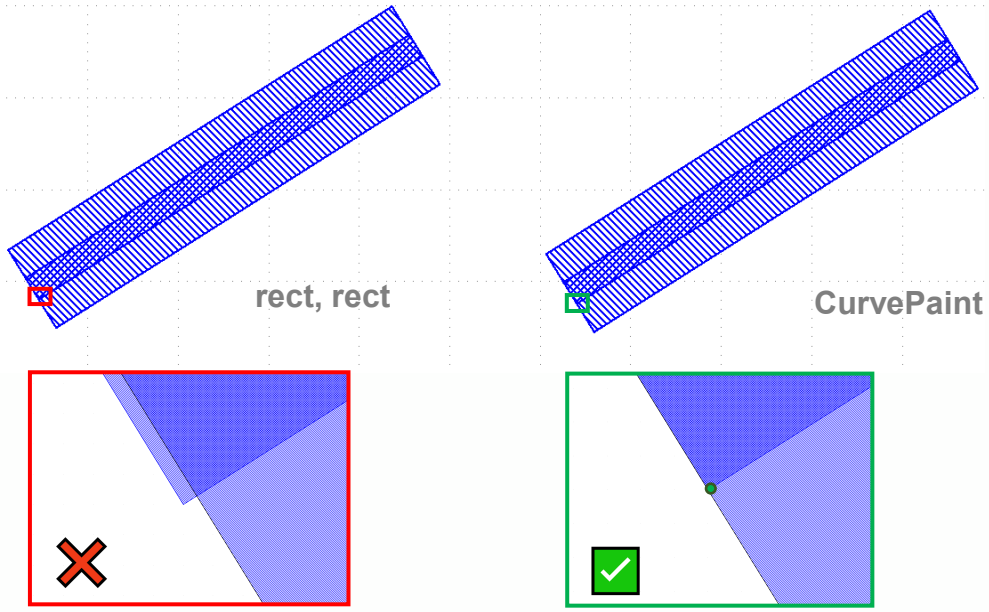
OK

LATITUDE DESIGN SYSTEMS

Maintaining Port and Core/Cladding Alignment

PhotoCAD supports unrestricted port angles, eliminating the need for manual angle constraints in design

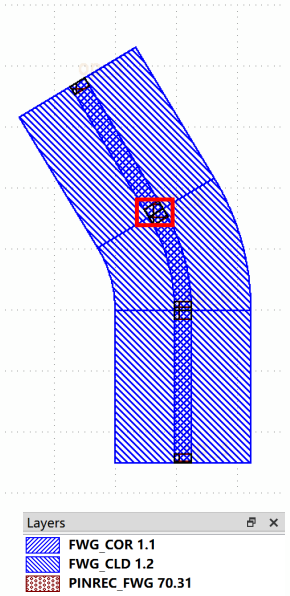
Use the **CurvePaint** method to avoid misalignments caused by point coordinate rounding



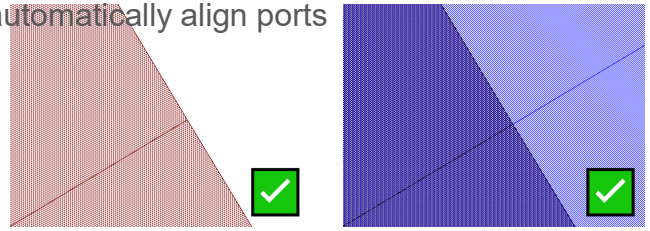
Rotating rectangles in waveguide construction causes coordinate rounding, which misaligns the core and cladding layers

CurvePaint maintains waveguide alignment during rotation and scaling operations

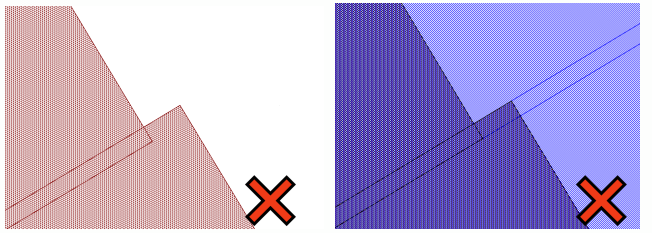
fp.export_gds automatically aligns ports by default



fp.export_gds(library, file=gds_file) # default
auto_flatten=True
#Flatten is enabled by default, and the output GDS will automatically align ports

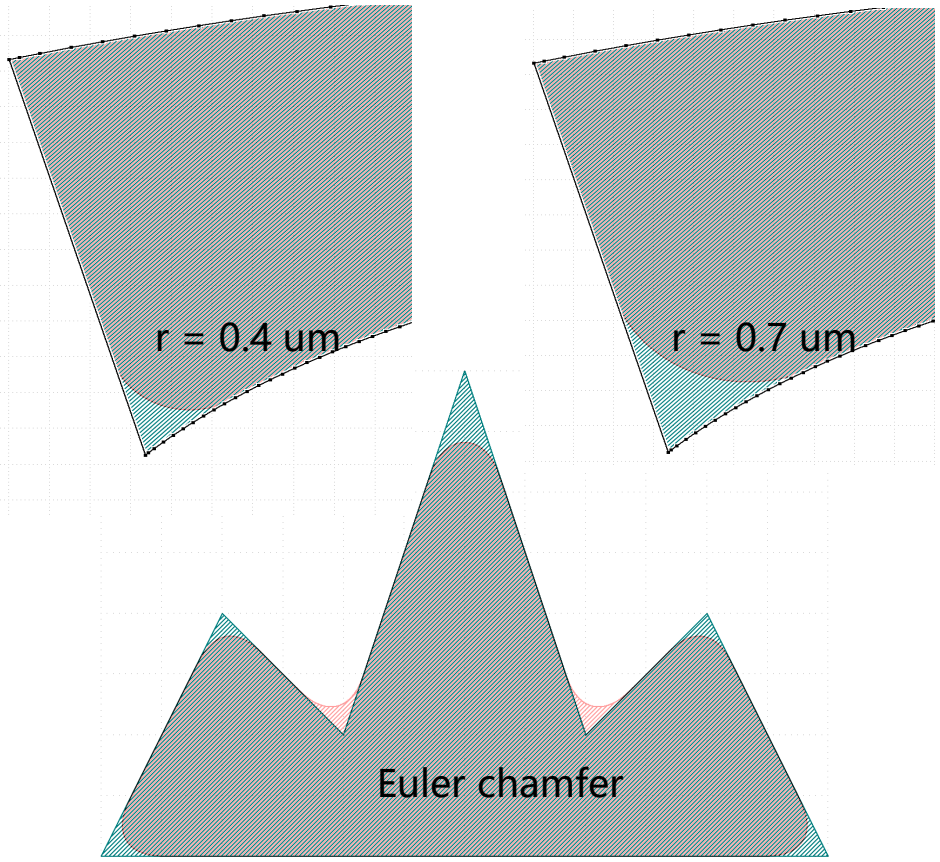


fp.export_gds(library, file=gds_file, **auto_flatten=False**)
#Disabling flatten prevents auto-alignment detection and requires manual fixes.

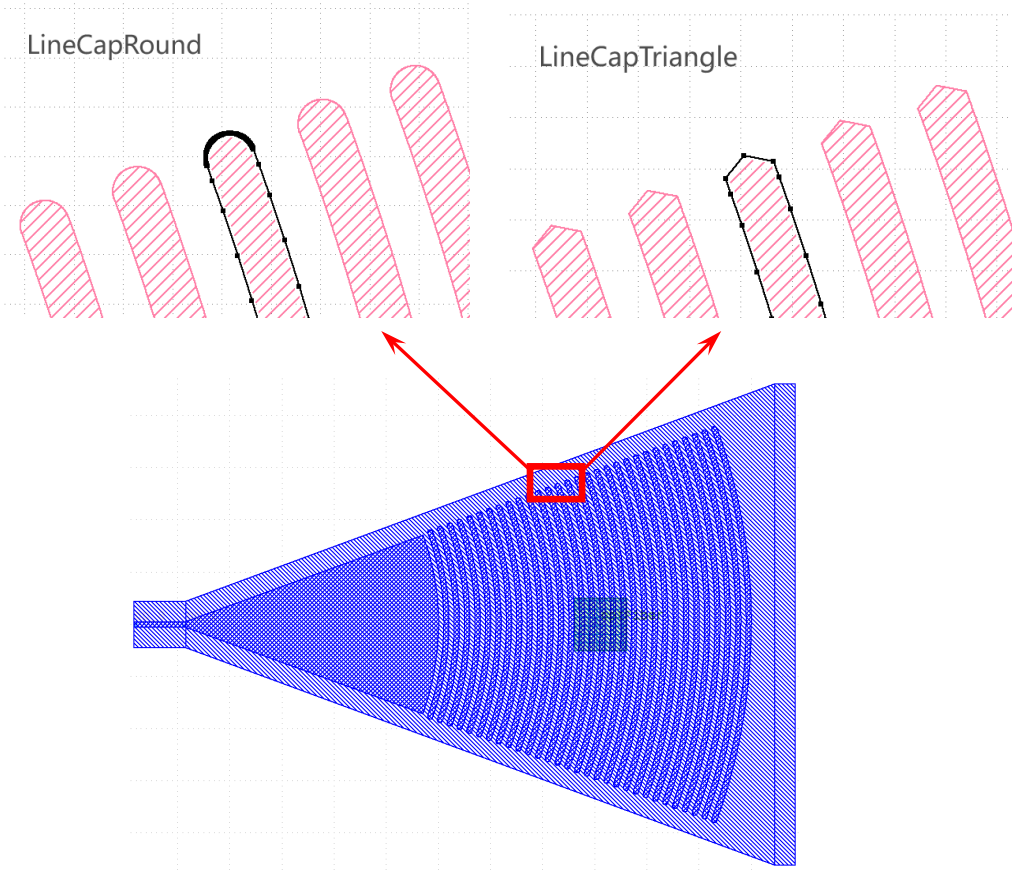


Fillet and Line Cap: Auto-Repair with Customizing Edge Treatments

1. Using **fillet**, you can control the radius of curvature/shape/critical angle of the chamfer

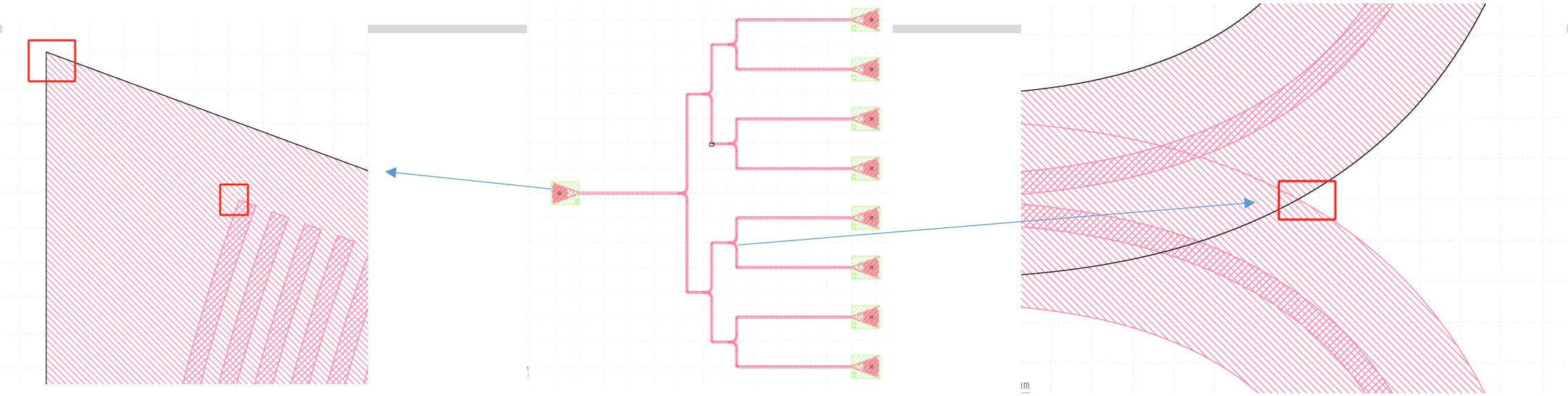


example：gpdk\examples\example_fillet.py



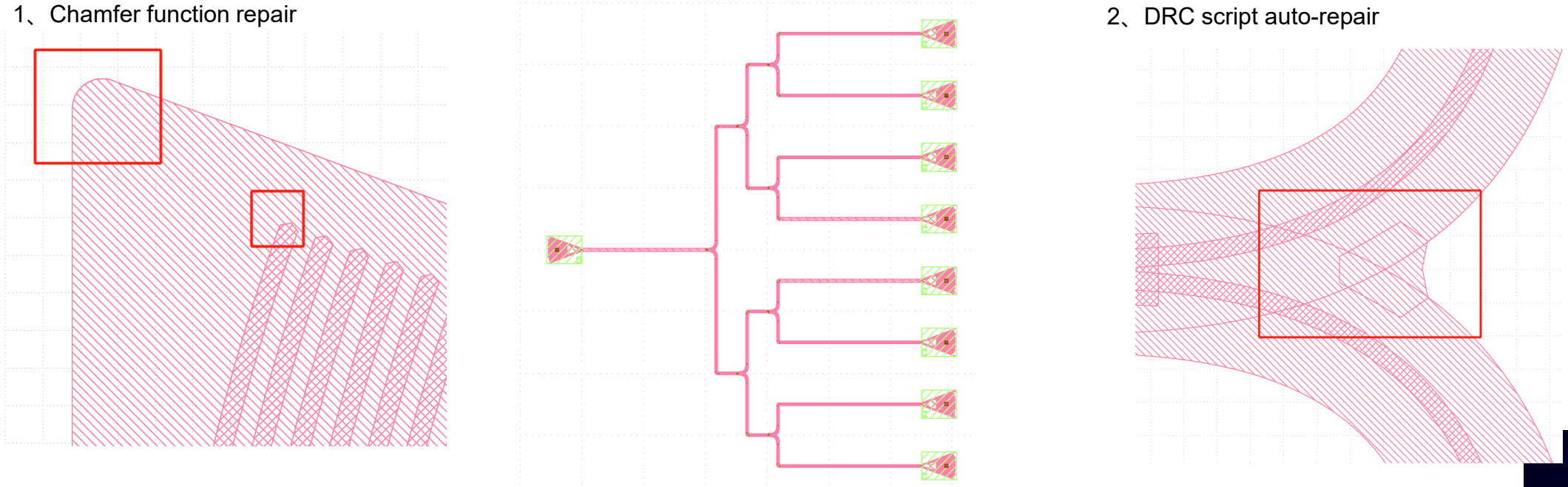
example：gpdk\examples\example_line_cap.py

Acute Angle Check and Automatic Repair



1、Chamfer function repair

2、DRC script auto-repair



pVerify DRC

Comprehensive Design Rule Verification

Design Accuracy & Compliance

Comprehensive design rule checking ensures photonic layouts meet foundry specifications through automated verification.

Real-Time Error Detection

Preliminary DRC checks during design enable immediate rule violation resolution before fabrication.

Seamless Integration

Integrates with existing PIC workflows providing intuitive verification without disrupting design methodology.

Ready to enhance your PIC design verification process?

Explore pVerify DRC

Key Capabilities

▶ Basic DRC Checks

- Minimum & Exact Width
- Spacing & Area Verification
- Layer Generation Methods
- Boolean Operations

▶ Advanced Geometry

- Enclosure & Separation
- Inside/Outside Checks
- Overlap Detection
- Acute Angle Analysis

▶ Density & Repair

- Local & Global Density
- Automatic Angle Patching
- Core/Cladding Alignment
- Custom Rule Support

Performance Benefits

- 90%+ Error Reduction
- 50%+ Time Savings

LATITUDE DESIGN SYSTEMS

PIC Studio

Complete Photonic Design Platform From Concept to Fabrication

40%+
Cost Reduction

30%+
Faster Development

100%
Unified Workflow

PhotoCAD
Advanced layout design & scripting

pSim Plus
System-level E/O simulation

Advanced SDL
Schematic-driven layout

pVerify DRC
Design rule verification

pMaxwell
FDTD component simulation

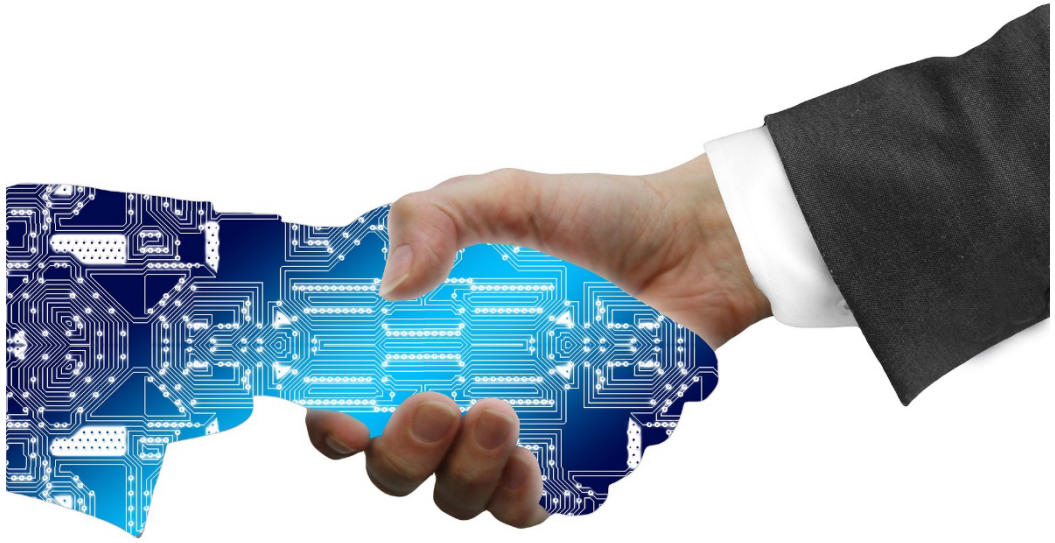
pLogic
Circuit simulation & control

Component Design & Simulation

Circuit Layout & Verification

System Integration & Testing

Fabrication & Assembly



Thank you

LATITUDE DESIGN SYSTEMS